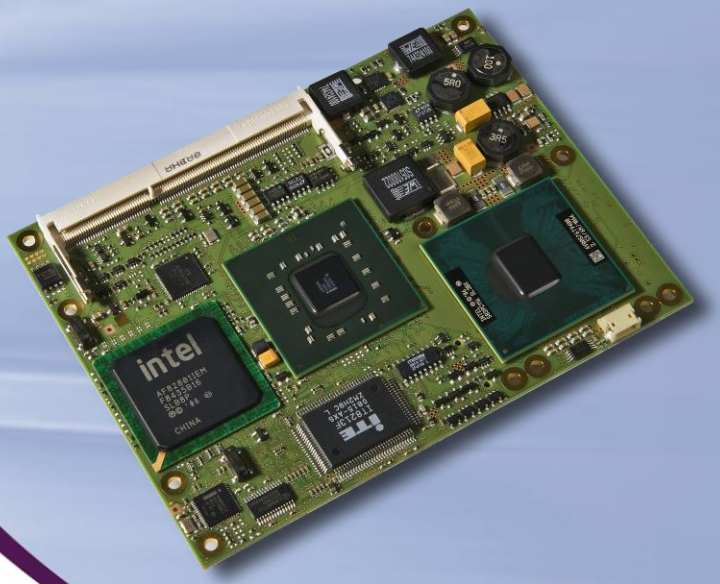
User's Manual



CXB-GM45

MSC COM Express™ Basic Module
Intel® Core™ 2 Duo

Rev. 1.3
February 18th, 2011

Preface

Copyright Notice

Important Information

This documentation is intended for qualified audience only. The product described herein is not an end user product. It was developed and manufactured for further processing by trained personnel.

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Although this document has been generated with the utmost care no warranty or liability for correctness or suitability for any particular purpose is implied. The information in this document is provided "as is" and is subject to change without notice.

EMC Rules

This unit has to be installed in a shielded housing. If not installed in a properly shielded enclosure, and used in accordance with the instruction manual, this product may cause radio interference in which case the user may be required to take adequate measures at his or her owns expense.

Trademarks

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Certification

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Life-Cycle-Management

MSC products are developed and manufactured according to high quality standards. Our life-cycle-management assures long term availability through permanent product maintenance. Technically necessary changes and improvements are introduced if applicable. A product-change-notification and end-of-life management process assures early information of our customers.

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MSC engineers and technicians are committed to provide support to our customers whenever needed.

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If the information provided there does not solve your problem, please contact our Technical Support:

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Content

1 General Information

1.1 Revision History

Rev.	Date	Description
1.0	Februar 12th,2010	Changed to Version 1.0.Bios chapter updated. Added PCI IRQ Routing table
1.1	June 10th 2010	Minor changes, new cover
1.2	Nov. 26th 2010	GPI2 and 3 – Pin changed (p. 25)
1.3	February 18th 2011	Corrected SMB Adresses

1.2 Reference Documents

[1] COM Express Module Base Specification
COM Express Revision 1.0
Last update: July 10th, 2005

[2] PCI Local Bus Specification Rev. 2.1
PCI21.PDF
Last update: June 1st, 1995
http://www.pcisig.com

[3] ATA/ATAPI-6 Specification
d1410r3b.pdf
http://www.t13.org/

[4] Serial ATA Specification
Serial ATA 1.0 gold.pdf
Last update: August 29th, 2002 Rev.1.0
http://www.sata-io.org/

[5] IEEE Std. 802.3-2002
802.3-2002.pdf
http://www.ieee.org

[6] Universal Bus Specification
usb_20.pdf
Last update: April 27th, 2000
http://www.usb.org

1.3 Introduction

COM Express™, an open specification of the PICMG (PCI Industrial Computer Manufacturer Group), is a module concept to bring PCI Express and other latest technologies like SATA, USB 2.0 and LVDS on a COM (Computer On Module).

A COM Express™ module is plugged onto an application-specific base board similar to the ETX concept, but offers more options and a growth path to future CPU technologies. Utilizing different sizes, COM Express™ can be used for highly embedded solutions up to high performance platforms.

The design of the MSC CXB-GM45 module supports the dual core CPU technology enabling you to boost your embedded application to highest performance levels.

For evaluation and design-in of the COM Express™ modules we offer evaluation baseboards and develop motherboards providing the interface infrastructure for the COM Express™ module using PC type connectors for external access.

Currently two module sizes are defined in the COM Express Specification 1.0: the Basic Module and the Extended Module. The primary difference between the Basic and the Extended Module is the over-all physical size and the performance envelope supported by each. The Extended Module is the largest and can support larger processor and memory solutions. The Basic Module is the most common supporting typical processor platforms in the embedded world.

All module sizes use the same connectors and pin-outs and utilize several common mounting hole positions. This level of compatibility allows that a carrier board designed to accommodate an Extended Module can also support a Basic Module.

Up to 440 pins of connectivity are available between COM Express™ modules and the Carrier Board. Legacy buses such as PCI, parallel ATA, LPC, HDA are supported as well as new high speed serial interconnects such as PCI Express, Serial ATA and Gigabit Ethernet.

To enhance interoperability between COM Express™ modules and Carrier Boards, five common signalling configurations (Pin-out Types) have been defined to ease system integration.

2 Technical Description

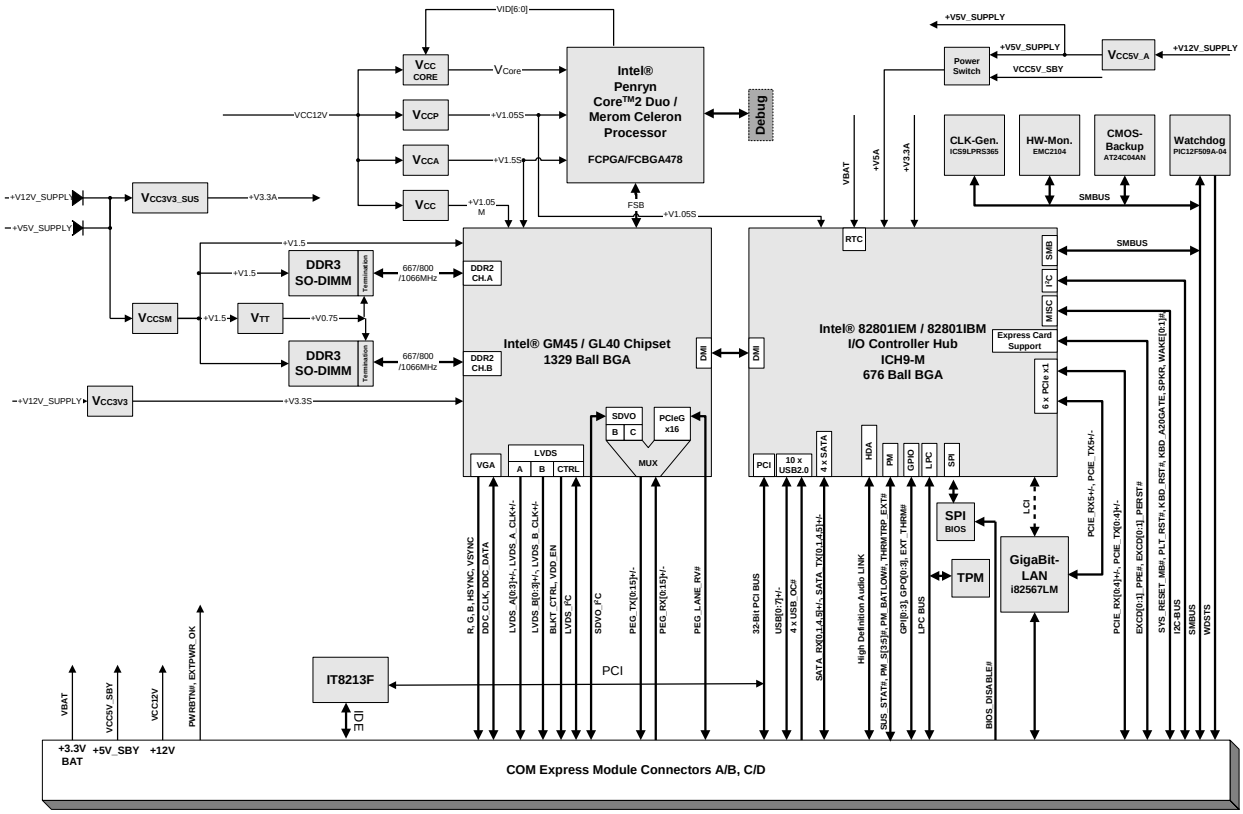
2.1 Key features

The MSC CXB-GM45 COM Express module is designed as a type 2 module.

Key features include:

- Module size: 125 mm x 95 mm
- 18 mm 'z' height with heat-spreader (with 5 mm stack option)
- Dual 220 pin connector (440 pins)
- 2x DDR3 SO-DIMM module
- Eight USB 2.0 ports; 4 shared over-current lines
- Four Serial ATA ports with data rates up to 3.0Gb/s (300MB/s)
- Five PCI Express x1 lanes
- Support pins for two ExpressCards
- One dual 24-bit LVDS channel
- Analog VGA
- High definition digital audio interface (external CODEC)
- Single GBit Ethernet interface
- LPC interface
- Four GPI pins
- Four GPO pins
- +12V primary power supply input
- +5V standby (optional) and 3.3V RTC power supply inputs
- 32 bit PCI interface
- IDE port (to support legacy ATA devices such as CD-ROM drives and Compact Flash storage cards)
- 21 PCI Express lanes (5 on A-B and 16 on C-D)
- 16 of 21 PCI Express lanes used for PCI Express Graphics
- SDVO option (pins shared with PCI Express Graphics)
- TPM module (option, TPM 1.2, SLB9635)
- Automatic fan control

2.2 Block diagram



2.3 COM Express implementation

COM Express™ required and optional features of pin-out type 2 are summarized in the following table. The features identified as Minimum (Min.) **shall** be implemented by all modules. Features identified up to Maximum (Max) **may** be additionally implemented by a module.

The column MSC CXB-GM45 shows the implemented features of the MSC module:

	Type 2	MSC CXB-GM45	Note
	Min / Max		
System I/O			
PCI Express Graphics (PEG)	0 / 1	1	signals are multiplexed with SDVO signals
PCI Express Lanes 0 - 5	2 / 6	5 (x1)	
PCI Express Lanes 16-31 (same as PEG pins)	0 / 16	1 (x16)	off-module x16 PCI Express Graphics
SDVO Channels	0 / 2	2	signals are multiplexed with PEG signals
LVDS Channels	0 / 2	2	1x dual channel, 2x24 Bit
VGA Port	0 / 1	1	
TV-Out	0 / 1	0	not implemented
PATA Port	1 / 1	1	

SATA Ports	2 / 4	4	
HDA Digital Interface	0 / 1	1	
USB 2.0 Ports	4 / 8	8	
Gbit LAN	1 / 1	1	
PCI Bus - 32 Bit	1 / 1	1	
Express Card Support	1 / 2	2	
LPC Bus	1 / 1	1	
System Management			
General Purpose Inputs	4 / 4	4	
General Purpose Outputs	4 / 4	4	
SMBus	1 / 1	1	
I2C	1 / 1	1	
Watch Dog Timer	0 / 1	1	
Speaker Out	1 / 1	1	
External BIOS ROM support	0 / 1	1	
Reset Functions	1 / 1	1	
Power Management			
Thermal Protection	0 / 1	1	
Battery Low Alarm	0 / 1	1	
Suspend	0 / 1	1	
Wake	0 / 2	2	
Power Button Support	1 / 1	1	
Power Good	1 / 1	1	
TPM	0 / 0	1	optional TPM 1.2 module

2.4 Functional units

CPUs	Intel® Celeron® 575 (Merom, Standard Voltage, 2.0GHz, FSB 667MHz, 478 PGA) Intel® Core™ 2 Duo T9400 (Penryn, Standard Voltage, 2.53 GHz, FSB 1066MHz, 478 PGA or 479 uBGA)
Chipset	Intel® GM45 or Intel® GL40 GMCH (Graphics Memory Controller Hub) Intel® ICH9M I/O Controller Hub
Memory	Two 204-pin DDR3 SO-DIMM sockets for up to 8GB (max. height 1250mil = 31.75mm) PC5300/6400/8500 DDR3 SDRAM (DDR667/800/1066)
SATA	4 SATA channels up to 300MByte/s each
EIDE	1 Enhanced IDE port ATA/UDMA100
USB	8 x USB 2.0
COM Express™	Type 2 interface, fully compliant
PCI Express™	Five channels PCIe x1
PCI	32 Bit standard interface
LPC	Low Pin Count Bus for heritage interfaces
Graphics Controller	Intel Gen 5.0 integrated graphics engine
Video Memory	Intel® Dynamic Video Memory Technology (Intel® DVMT 5.0)
LCD Interface	LVDS 2x24Bit, dual channel, max. resolution 1.600 x 1.200
SDVO Interface	2 independent SDVO interfaces (SDVOB, SDVOC) or external PCIe x16 graphics (multiplexed by Intel Gen 5.0 integrated graphics engine)
CRT Interface	max. resolution 2.048 x 1.536
Ethernet	10/100/1000Base-TX (Intel® 82567L)
Sound Interface	High Definition Audio Interface
Watchdog Timer	PIC12C509A Creates system reset (programmable, 1s ... 255h)
TPM (option)	Optional TPM module, TPM 1.2, SLB9635
Fan Supply	3-pin header (12V)
Real Time Clock (RTC)	integrated in ICH9M
Battery	External
System Monitoring	Voltage , Temperature , Fan ▪ Core voltage ▪ 12V ▪ CPU thermal diode ▪ RAM Temperature ▪ System Temperature ▪ Automatic Fan Control

2.5 System Memory

The MSC CXB-GM45 CPU module provides two sockets for memory modules which have to meet the following demands:

- 204pin unbuffered DDR3 SO-DIMM
- 1.5V Supply Voltage
- DDR3-800 / PC3-6400 or faster; for CPUs with a 1066MHz FSB frequency DDR3-1066 / PC3-8500 is highly recommended
- Max. Module height: 30mm
- SPD (Serial Presence Detect) EEPROM

The CPU module provides a Management Engine from Intel®, which has access exclusively to memory channel A; which again is connected to the memory socket on the upper side (usually below the heat sink). This means that if only one memory module is used, it should be installed into the upper socket (The CPU module will boot and work normally with only one memory module installed in the socket at the back side of the module; anyway, the Intel® Management Engine will not work. This might cause unexpected behavior in some applications).

Anyway, the best performance will be achieved with both memory sockets equipped with equal memory modules.

2.6 Power Supply

- **+12V primary power supply input**
- **+5V standby**
  Option, is not required for module operation.
  If not present, customer has to make sure that the supply voltages which are generated on the carrier board are switched off during suspend states, so that no current from the carrier board's signal lines can flow to the CPU board.
- **3.3V RTC power supply**
  Option, is not required for module operation.
  BIOS SETUP data is stored in a non volatile backup memory device (EEPROM), therefore configuration data will not get lost during power off (except for time and date information)

Voltage	Input range	Current
+12V	+11.4V - 12.6 V	See next table
+5V Standby	+4.75V - 5.25 V	max. 2A
+3V RTC power supply	+2.0V - 3.3V	max. 6µA

2.7 Current Dissipation

All measurements were made by plugging a MSC CXB-GM45 Module onto a MSC CX-EVA2 Baseboard with a Multimeter connected to the +12V Line. The module was equipped with two 2GByte memory modules Hynix HMT125S6AFP8C-G7 No AA-C, 2GB 2Rx8 PC3-8500S-7-10-F1.

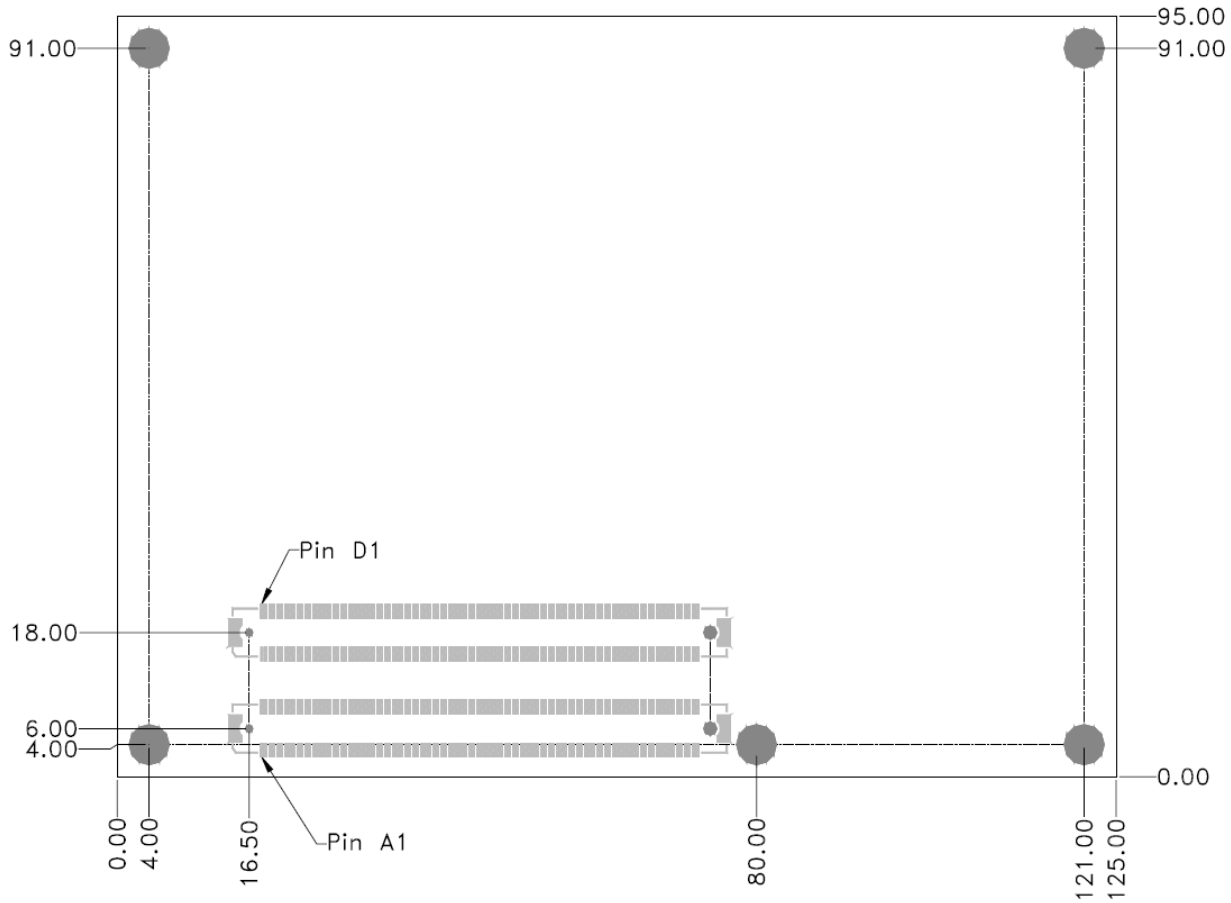
Three tests were performed:

1. Booting Dos 6.22 from an USB stick
2. Booting Microsoft Windows XP Professional SP3 from an IDE harddrive to the desktop
3. Booting Mocrosoft Windows XP Professional SP3 from an IDE harddrive and using Intel Thermal Analysis Tool (V. 3.8.0.1012) to achieve 100% CPU load.

Module (CPU)	DOS Prompt	Windows XP Idle	100% CPU load
Intel® Core™2 Duo T9400 2.53GHz, 1066MHz FSB, 3M Cache	1.7A	0.7A	4.0A
Intel® Core™2 Duo P8400 2.26GHz, 1066MHz FSB, 3M Cache	1.7A	0.7A	3.7A
Intel® Pentium® T4200 2.0GHz, 800MHz FSB, 1M Cache	1.5A	0.75A	3.3A
Intel® Celeron Dual Core T3100 1.9GHz, 800MHz FSB, 1M Cache	1.6A	0.9A	3.6A
Intel® Celeron 575	1.75A	1.1A	2,7A

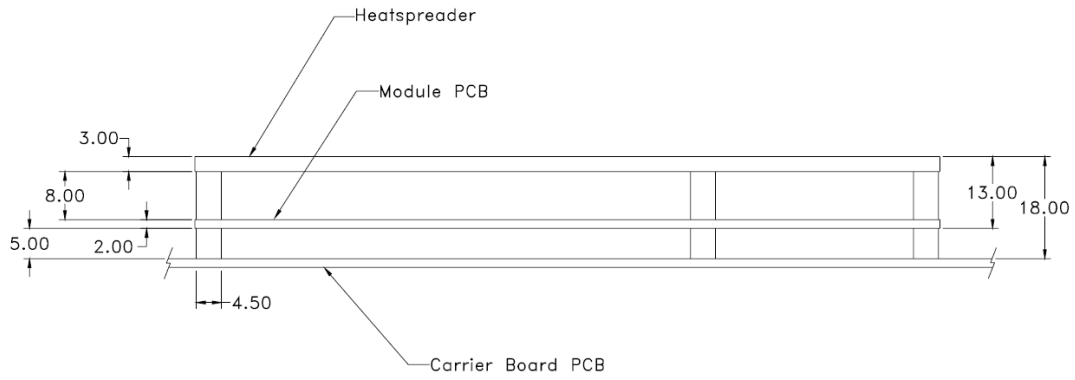
2.8 Mechanical Dimensions

2.8.1 Compact module



There are two height options defined in the COM Express specification : 5mm and 8mm.

The height option is defined by the connectors on the baseboard.



2.9 Thermal specifications

The cooling solution of a COM Express module is based on a heatspreader concept.

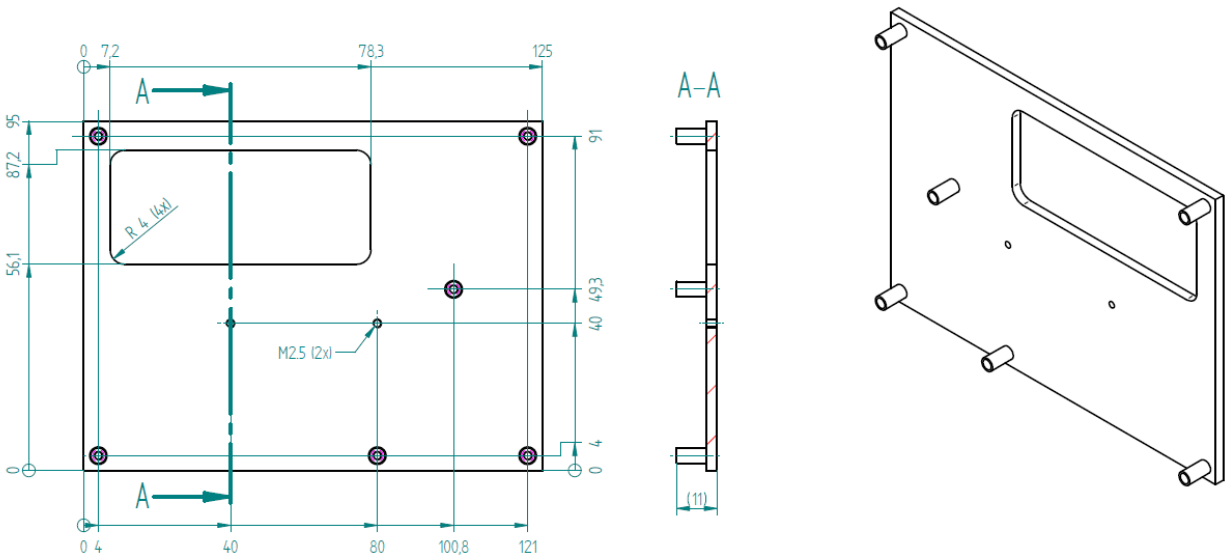
A heatspreader is a metal plate (typically aluminium) mounted on the top of the module. The connection between this plate and the module components is typically done by thermal interface materials like phase change foils, gap pads and copper or aluminium blocks. A very good thermal conductivity is required in order to conduct the heat from the cpu and the chipset to the heatspreader plate.

The heatspreader of the MSC module is thermally attached using phase change materials and small aluminium blocks filling the gap between cpu and chipset dies and the heatspreader plate.

The heatspreader is not a heatsink! It is a defined thermal interface for the system designer with fixed mechanical dimensions, so it should be possible to change different module types without problems. There must be a cooling solution for the system, the surface temperature of the heatspreader should not exceed 80°C .

Main issue for the thermal functionality of a system is that each device of the module is operated within its specified thermal values. The max values of CPU and chipset are 100°C, so there may be system implementations where the heatspreader temperature could be higher.

Anyway, in this case it has to be validated that there are no thermal spec violations of any assembled part or integrated circuit over the system temperature range even at worst case conditions.



2.10 Signal description

Pins are marked in the following tables with the power rail associated with the pin, and, for input and I/O pins, with the input voltage tolerance. The pin power rail and the pin input voltage tolerance **may** be different. For example, the PCI group is defined as having a 3.3V power rail, meaning that the output signals will only be driven to 3.3V, but the pins are tolerant of 5V signals.

An additional label, "Suspend", indicates that the pin is active during suspend states (S3,S4,S5). If suspend modes are used, then care must be taken to avoid loading signals that are active during suspend to avoid excessive suspend mode current draw.

2.10.1 High Definition Audio

Signal	Pin Type	Signal Level	Power Rail	Power Tolerance	PU/PD	Description	Source / Target
AC_RST#	Output	CMOS	3.3V Sus.	3.3V	20k PD	Reset output to CODEC, active low.	ICH9M
AC_SYNC	Output	CMOS	3.3V	3.3V	20k PD	48kHz fixed-rate, sample-synchronization signal to the CODEC(s).	ICH9M
AC_BITCLK	Output	CMOS	3.3V	3.3V	20k PD	24.00 MHz serial data clock generated by the ICH9-M	ICH9M
AC_SDOUT	Output	CMOS	3.3V	3.3V	20k PD	Serial TDM data output to the CODEC.	ICH9M
AC_SDIN[0:2]	Input	CMOS	3.3V Sus.	3.3V	20k PD	Serial TDM data inputs from up to 3 CODECs.	ICH9M

2.10.2 Ethernet

Signal	Pin Type	Signal Level	Power Rail	Power Tolerance	PU/PD	Description	Source / Target
GBE0_MDI[0:3]+ GBE0_MDI[0:3]-	Input/ Output	Analog	3.3V Sus.			Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. MDI[0]+/- B1_DA+/- MDI[1]+/- B1_DB+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	82567L
GBE0_ACT#	Open Drain	CMOS	3.3V Sus.	3.3V		Gigabit Ethernet Controller 0 activity indicator, active low.	82567L
GBE0_LINK#	Open Drain	CMOS	3.3V Sus.	3.3V		Gigabit Ethernet Controller 0 link indicator, active low.	82567L
GBE0_LINK100#	Open Drain	CMOS	3.3V Sus.	3.3V		Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	82567L
GBE0_LINK1000#	Open Drain	CMOS	3.3V Sus.	3.3V		Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	82567L

Signal	Pin Type	Signal Level	Power Rail	Power Tolerance	PU/PD	Description	Source / Target
GBE0_CTREF	REF			GND min 3.3V max		82567 (1000MBit) : 1,8V	82567L

2.10.3 IDE

Signal	Pin Type	Signal Level	Power Rail	Power Tolerance	PU/PD	Description	Source / Target
IDE_D[0:6,8:15]	I/O	CMOS	3.3V	5V		Bidirectional data to / from IDE device.	IT8213F
IDE_D[7]	I/O	CMOS	3.3V	5V	10k PD	Bidirectional data to / from IDE device.	IT8213F
IDE_A[0:2]	O	CMOS	3.3V	3.3V		Address lines to IDE device.	IT8213F
IDE_IOW#	O	CMOS	3.3V	3.3V		I/O write line to IDE device. Data latched on trailing (rising) edge.	IT8213F
IDE_IOR#	O	CMOS	3.3V	3.3V		I/O read line to IDE device.	IT8213F
IDE_REQ	I	CMOS	3.3V	5V	5k6 PD	IDE Device DMA Request. It is asserted by the IDE device to request a data transfer.	IT8213F
IDE_ACK#	O	CMOS	3.3V	3.3V		IDE Device DMA Acknowledge.	IT8213F
IDE_CS1#	O	CMOS	3.3V	3.3V		IDE Device Chip Select for 1Foh to 1FFh range.	IT8213F
IDE_CS3#	O	CMOS	3.3V	3.3V		IDE Device Chip Select for 3Foh to 3FFh range.	IT8213F
IDE_IORDY	I	CMOS	3.3V	5V	1k PU	IDE device I/O ready input. Pulled low by the IDE device to extend the cycle.	IT8213F
IDE_RESET#	O	CMOS	3.3V	3.3V		Reset output to IDE device, active low.	IT8213F
IDE_IRQ	I	CMOS	3.3V	5V	10k PD	Interrupt request from IDE device.	IT8213F
IDE_CBLID#	I	CMOS	3.3V	5V		Input from off-module hardware indicating the type of IDE cable being used. High indicates a 40-pin cable used for legacy IDE modes. Low indicates that an 80-pin cable with interleaved grounds is used. Such a cable is required for Ultra-DMA 66, 100 and 133 modes.	IT8213F

2.10.4 Serial ATA

Signal	Pin Type	Signal Level	Power Rail	Remark	PU/PD	Description	Source / Target
SATA0_TX+ SATA0_TX-	O	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 transmit differential pair.	ICH9M
SATA0_RX+ SATA0_RX-	I	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 receive differential pair.	ICH9M
SATA1_TX+ SATA1_TX-	O	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 transmit differential pair.	ICH9M

Signal	Pin Type	Signal Level	Power Rail	Remark	PU/PD	Description	Source / Target
SATA1_RX+ SATA1_RX-	I	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 receive differential pair.	ICH9M
SATA2_TX+ SATA2_TX-	O	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 transmit differential pair.	ICH9M
SATA2_RX+ SATA2_RX-	I	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 receive differential pair.	ICH9M
SATA3_TX+ SATA3_TX-	O	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 transmit differential pair.	ICH9M
SATA3_RX+ SATA3_RX-	I	SATA	3.3V	AC coupled on module		Serial ATA Channel 0 receive differential pair.	ICH9M
ATA_ACT#	O	CMOS	3.3V	3.3V		SATA activity indicator, active low.	ICH9M

2.10.5 PCI Express Lanes

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
PCIE_TX[0:4]+ PCIE_TX[0:4]-	O	PCIe	3.3V	AC coupled on module		PCI Express Differential Transmit Pairs 0 through 4	ICH9M
PCIE_RX[0:4]+ PCIE_RX[0:4]-	I	PCIe	3.3V	AC coupled off module		PCI Express Differential Receive Pairs 0 through 4	ICH9M
PCIE_TX[5]+ PCIE_TX[5]-	O	PCIe	3.3V	AC coupled on module		PCI Express Differential Transmit Pair 5	not supported
PCIE_RX[5]+ PCIE_RX[5]-	I	PCIe	3.3V	AC coupled off module		PCI Express Differential Receive Pair 5	not supported
PCIE_TX[16:31]+ PCIE_TX[16:31]-	O	PCIe	3.3V	AC coupled on module		PCI Express Differential Transmit Pairs 16 through 31. These are same lines as PEG_TX[0:15]+ and - in module pin-out types 4 and 5.	GM45
PCIE_RX[16:31]+ PCIE_RX[16:31]-	I	PCIe	3.3V	AC coupled off module		PCI Express Differential Receive Pairs 16 through 31. These are the same lines as PEG_RX[0:15]+ and - in module pin-out types 4 and 5.	GM45
PCIE_CLK_REF+ PCIE_CLK_REF-	O	PCIe CLK	3.3V	AC coupled on module		Reference clock output for all PCI Express and PCI Express Graphics lanes.	CK505

2.10.6 PCI Express Lanes x16

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
PEG_TX[0:15]+ PEG_TX[0:15]-	O	PCIe	3.3V	AC coupled on module		PCI Express Graphics transmit differential pairs. Some of these are multiplexed with SDVO lines (see SDVO section). These are the same lines as PCIE_TX[16:31]+ and - in module pin-out types 4 and 5.	GM45
PEG_RX[0:15]+ PEG_RX[0:15]-	I	PCIe	3.3V	AC coupled off module		PCI Express Graphics receive differential pairs. Some of these are multiplexed with SDVO lines (see SDVO section). These are the same lines as PCIE_RX[16:31]+ and - in module pin-out types 4 and 5.	GM45
PEG_LANE_RV#	I	CMOS	3.3V	3.3V	5k7 PU	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order. Be aware that the SDVO lines that share this interface do not necessarily reverse order if this strap is low.	GM45 (CFG 9)
PEG_ENABLE#	I	CMOS	3.3V	3.3V	100k PU	Strap to enable PCI Express x16 external graphics interface. Pull low to disable internal graphics and enable the x16 interface.	ICH9M (GPI17)

2.10.7 Express Card Support

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
EXCD[0]_CPPE#	I	CMOS	3.3V	3.3V	8k2 PU	ExpressCard card request, active low	ICH9M
EXCD[1]_CPPE#	I	CMOS	3.3V	3.3V		ExpressCard card request, active low	ICH9M
EXCD[0]_RST#	O	CMOS	3.3V	3.3V	8k2 PU	ExpressCard reset, active low	ICH9M
EXCD[1]_RST#	O	CMOS	3.3V	3.3V	8k2 PU	ExpressCard reset, active low	ICH9M

2.10.8 PCI Bus

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
PCI_AD[0:31]	I/O	CMOS	3.3V	5V		PCI bus multiplexed address and data lines	ICH9M
PCI_C/BE[0:3]#	I/O	CMOS	3.3V	5V		PCI bus byte enable lines, active low	ICH9M
PCI_DEVSEL#	I/O	CMOS	3.3V	5V	8k2 PU	PCI bus Device Select, active low.	ICH9M
PCI_FRAME#	I/O	CMOS	3.3V	5V	8k2 PU	PCI bus Frame control line, active low.	ICH9M
PCI_IRDY#	I/O	CMOS	3.3V	5V	8k2 PU	PCI bus Initiator Ready control line, active low.	ICH9M
PCI_TRDY#	I/O	CMOS	3.3V	5V	8k2 PU	PCI bus Target Ready control line, active low.	ICH9M
PCI_STOP#	I/O	CMOS	3.3V	5V	8k2 PU	PCI bus STOP control line, active low, driven by cycle initiator.	ICH9M
PCI_PAR	I/O	CMOS	3.3V	5V		PCI bus parity	ICH9M
PCI_PERR#	I/O	CMOS	3.3V	5V	8k2 PU	Parity Error: An external PCI device drives PERR# when it receives data that has a parity error.	ICH9M
PCI_REQ[0:2]#	I	CMOS	3.3V	5V	8k2 PU	PCI bus master request input lines, active low.	ICH9M
PCI_GNT[0:2]#	O	CMOS	3.3V	5V		PCI bus master grant output lines, active low.	ICH9M
PCI_REQ[3]#	I	CMOS	3.3V	5V	75k PU	PCI bus master request input lines, active low.	IT8208M
PCI_GNT[3]#	O	CMOS	3.3V	5V		PCI bus master grant output lines, active low.	IT8208M
PCI_RESET#	O	CMOS	3.3V Sus.	5V		PCI Reset output, active low.	ICH9M
PCI_LOCK#	I/O	CMOS	3.3V	5V	8k2 PU	PCI Lock control line, active low.	ICH9M
PCI_SERR#	I/O OD	CMOS	3.3V	5V	8k2 PU	System Error: SERR# may be pulsed active by any PCI device that detects a system error condition.	ICH9M
PCI_PME#	I	CMOS	3.3V Sus.	5V	20k PU	PCI Power Management Event: PCI peripherals drive PME# to wake system from low-power states S1–S5.	ICH9M
PCI_CLKRUN#	I/O	CMOS	3.3V	5V	8k2 PU	Bidirectional pin used to support PCI clock run protocol for mobile systems.	ICH9M
PCI_IRQ[A:D]#	I	CMOS	3.3V	5V	8k2 PU	PCI interrupt request lines.	ICH9M
PCI_CLK	O	CMOS	3.3V	3.3V	10k PD	PCI 33MHz clock output.	CK505
PCI_M66EN	I	CMOS	3.3V	5V		Module input signal indicates whether an off-module PCI device is capable of 66MHz operation. Pulled to GND by Carrier Board device or by Slot Card if the devices are NOT capable of 66 MHz operation. If the module is not capable of supporting 66 MHz PCI operation, this input may be a no-connect on the module. If the module is capable of supporting 66 MHz PCI operation, and if this input is held low by the Carrier Board, the module PCI interface shall operate at 33 MHz.	Not supported

2.10.9 USB

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
USB[0:7]+ USB[0:7]-	I/O	USB	3.3V Sus.	3.3V		USB differential pairs, channels 0 through 7	ICH9M
USB_0_1_OC#	I	CMOS	3.3V Sus.	3.3V	8k2 PU	USB over-current sense, USB channels 0 and 1. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	ICH9M
USB_2_3_OC#	I	CMOS	3.3V Sus.	3.3V	8k2 PU	USB over-current sense, USB channels 2 and 3. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	ICH9M
USB_4_5_OC#	I	CMOS	3.3V Sus.	3.3V	8k2 PU	USB over-current sense, USB channels 4 and 5. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	ICH9M
USB_6_7_OC#	I	CMOS	3.3V Sus.	3.3V	8k2 PU	USB over-current sense, USB channels 6 and 7. A pull-up for this line is present on the module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	ICH9M

2.10.10 LVDS Flat Panel

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
LVDS_A[0:3]+ LVDS_A[0:3]-	O	LVDS				LVDS Channel A differential pairs	GM45
LVDS_A_CK+ LVDS_A_CK-	O	LVDS				LVDS Channel A differential clock	GM45
LVDS_B[0:3]+ LVDS_B[0:3]-	O	LVDS				LVDS Channel B differential pairs	GM45
LVDS_B_CK+ LVDS_B_CK-	O	LVDS				LVDS Channel B differential clock	GM45
LVDS_VDD_EN	O	CMOS	3.3V	3.3V	100k PD	LVDS panel power enable	GM45
LVDS_BKLT_EN	O	CMOS	3.3V	3.3V	100k PD	LVDS panel backlight enable	GM45
LVDS_BKLT_CTRL	O	CMOS	3.3V	3.3V		LVDS panel backlight brightness control	GM45

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
LVDS_I2C_CK	O	CMOS	3.3V	3.3V	2k2 PU	I2C clock output for LVDS display use	GM45
LVDS_I2C_DAT	I/O OD	CMOS	3.3V	3.3V	2k2 PU	I2C data line for LVDS display use	GM45

2.10.11 LPC Bus

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
LPC_AD[0:3]	I/O	CMOS	3.3V	3.3V		LPC multiplexed address, command and data bus	ICH9M
LPC_FRAME#	O	CMOS	3.3V	3.3V		LPC frame indicates the start of an LPC cycle	ICH9M
LPC_DRQ[0:1]#	I	CMOS	3.3V	3.3V	20k PU	LPC serial DMA request	ICH9M
LPC_SERIRQ	I/O	CMOS	3.3V	3.3V		LPC serial interrupt	ICH9M
LPC_CLK	O	CMOS	3.3V	3.3V		LPC clock output - 33MHz nominal	CK505

2.10.12 Analog VGA

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
VGA_RED	O	Analog			150R PD	Red for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	GM45
VGA_GRN	O	Analog			150R PD	Green for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	GM45
VGA_BLU	O	Analog			150R PD	Blue for monitor. Analog DAC output, designed to drive a 37.5-Ohm equivalent load.	GM45
VGA_HSYNC	O	CMOS	3.3V	3.3V		Horizontal sync output to VGA monitor	GM45
VGA_VSYNC	O	CMOS	3.3V	3.3V		Vertical sync output to VGA monitor	GM45
VGA_I2C_CK	O	CMOS	3.3V	3.3V	2k2 PU	DDC clock line (I2C port dedicated to identify VGA monitor capabilities)	GM45
VGA_I2C_DAT	I/O OD	CMOS	3.3V	3.3V	2k2 PU	DDC data line.	GM45

2.10.13 TV Out

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
TV_DAC_A	O	Analog				TVDAC Channel A Output supports the following: ▪ Composite video: not used ▪ CVBS Component video: Chrominance (Pb) analog signal ▪ S-Video: not used	Not supported
TV_DAC_B	O	Analog				TVDAC Channel B Output supports the following: ▪ Composite video: not used ▪ Component video: Luminance (Y) analog signal ▪ S-Video: Luminance analog signal.	Not supported
TV_DAC_C	O	Analog				TVDAC Channel C Output supports the following: ▪ Composite video: not used ▪ Component: Chrominance (Pr) analog signal. ▪ S-Video: Chrominance analog signal.	Not supported

2.10.14 SVDO

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
SDVOB_RED+ SDVOB_RED-	O	PCIe		AC coupled on module		Serial Digital Video B red output differential pair Multiplexed with PEG_TX[0]+ and PEG_TX[0]- pair	GM45
SDVOB_GRN+ SDVOB_GRN-	O	PCIe		AC coupled on module		Serial Digital Video B green output differential pair Multiplexed with PEG_TX[1]+ and PEG_TX[1]-	GM45
SDVOB_BLU+ SDVOB_BLU-	O	PCIe		AC coupled on module		Serial Digital Video B blue output differential pair Multiplexed with PEG_TX[2]+ and PEG_TX[2]-	GM45
SDVOB_CK+ SDVOB_CK-	O	PCIe		AC coupled on module		Serial Digital Video B clock output differential pair. Multiplexed with PEG_TX[3]+ and PEG_TX[3]-	GM45
SDVOB_INT+ SDVOB_INT-	I	PCIe		AC coupled off module		Serial Digital Video B interrupt input differential pair. Multiplexed with PEG_RX[1]+ and PEG_RX[1]-	GM45
SDVOC_RED+ SDVOC_RED-	O	PCIe		AC coupled on module		Serial Digital Video C red output differential pair. Multiplexed with PEG_TX[4]+ and PEG_TX[4]-	GM45
SDVOC_GRN+ SDVOC_GRN-	O	PCIe		AC coupled on module		Serial Digital Video C green output differential pair. Multiplexed with PEG_TX[5]+ and PEG_TX[5]-	GM45
SDVOC_BLU+ SDVOC_BLU-	O	PCIe		AC coupled on module		Serial Digital Video C blue output differential pair. Multiplexed with PEG_TX[6]+ and PEG_TX[6]-	GM45
SDVOC_CK+ SDVOC_CK-	O	PCIe		AC coupled on module		Serial Digital Video C clock output differential pair. Multiplexed with PEG_TX[7]+ and PEG_TX[7]-	GM45

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
SDVOC_INT+ SDVOC_INT-	I	PCIe		AC coupled off module		Serial Digital Video C interrupt input differential pair. Multiplexed with PEG_RX[5]+ and PEG_RX[5]-	GM45
SDVO_TVCLKIN+ SDVO_TVCLKIN-	I	PCIe		AC coupled off module		Serial Digital Video TVOUT synchronization clock input differential pair. Multiplexed with PEG_RX[0]+ and PEG_RX[0]-	Not supported
SDVO_FLDSTALL+ SDVO_FLDSTALL-	I	PCIe		AC coupled off module		Serial Digital Video Field Stall input differential pair. Multiplexed with PEG_RX[2]+ and PEG_RX[2]-	GM45
SDVO_I2C_CK	O	CMOS	2.5V	2.5V		SDVO I2C clock line - to set up SDVO peripherals.	GM45
SDVO_I2C_DAT	I/O OD	CMOS	2.5V	2.5V		SDVO I2C data line - to set up SDVO peripherals.	GM45

2.10.15 Miscellaneous

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
I2C_CK	O	CMOS	3.3V	3.3V	2k2 PU	General purpose I2C port clock output	ICH9M / GPIO13
I2C_DAT	I/O	CMOS	3.3V	3.3V	2k2 PU	General purpose I2C port data I/O line	ICH9M / GPIO18
SPKR	O	CMOS	3.3V	3.3V	20k PD	Output for audio enunciator - the "speaker" in PC-AT systems	ICH9M
BIOS_DISABLE#	I	CMOS	3.3V	3.3V	100k PU	Module BIOS disable input. Pull low to disable module BIOS.	Disables SPI Flash
WDT	O	CMOS	3.3V	3.3V		Output indicating that a watchdog time-out event has occurred.	PIC12C509
KBD_RST#	I	CMOS	3.3V	3.3V	10k PU	Input to module from (optional) external keyboard controller that can force a reset. Pulled high on the module. This is a legacy artifact of the PC-AT.	ICH9M
KBD_A20GATE		CMOS	3.3V	3.3V	10k PU	Input to module from (optional) external keyboard controller that can be used to control the CPU A20 gate line. The A20GATE restricts the memory access to the bottom megabyte and is a legacy artifact of the PC- AT. Pulled high on the module.	ICH9M

2.10.16 Power and System Management

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
PWRBTN#	I	CMOS	3.3V Sus.	3.3V	20k PU	Power button to bring system out of Suspend states, active on falling edge.	ICH9M

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
SYS_RESET#	I	CMOS	3.3V Sus.	3.3V	10k PU	Reset button input. When the SYS_RESET# pin is detected as active after the 16 ms debounce logic, the ICH attempts to perform a "graceful" reset, by waiting up to 25 ms for the SMBus to go idle. If the SMBus is idle when the pin is detected active, the reset occurs immediately; otherwise, the counter starts. If at any point during the count the SMBus goes idle the reset occurs. If, however, the counter expires and the SMBus is still active, a reset is forced upon the system even though activity is still occurring. Once the reset is asserted, it remains asserted for 5 to 6 ms regardless of whether the SYS_RESET# input remains asserted or not. It cannot occur again until SYS_RESET# has been detected inactive after the debounce logic, and the system is back to a full So state. This behavior is a result of Intel ICH internal chipset logic which is different to the COM Express Module Base Specification stating that the system shall remain in reset as long as SYS_RESET# input is low.	ICH9M
CB_RESET#	O	CMOS	3.3V Sus.	3.3V	100k PD	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the module software.	ICH9M, GM45, FWH, LAN, TPM
PWR_OK	I	CMOS	3.3V Sus.	3.3V	100k PU	Power OK from main power supply. A high value indicates that the power is good.	Power Good logic
SUS_STAT#	O	CMOS	3.3V Sus.	3.3V		Indicates imminent suspend operation; used to notify LPC devices.	ICH9M
SUS_S3#	O	CMOS	3.3V Sus.	3.3V		Indicates system is in Suspend to RAM state. Active low output.	ICH9M
SUS_S4#	O	CMOS	3.3V Sus.	3.3V		Indicates system is in Suspend to Disk state. Active low output.	ICH9M
SUS_S5#	O	CMOS	3.3V Sus.	3.3V		Indicates system is in Soft Off state. Also known as "PS_ON" and can be used to control an ATX power supply.	ICH9M
WAKE0#	I	CMOS	3.3V Sus.	3.3V	10k PU	PCI Express wake up signal.	ICH9M
WAKE1#	I	CMOS	3.3V Sus.	3.3V	10k PU	General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.	ICH9M GPIO14
BATLOW#	I	CMOS	3.3V Sus.	3.3V	8k2 PU	Indicates that external battery is low.	ICH9M
THRM#	I	CMOS	3.3V	3.3V	10k PU	Input from off-module temp sensor indicating an over-temp situation.	ICH9M GPIO48

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
THERMTRIP#	O	CMOS	3.3V	3.3V		Active low output indicating that the CPU has entered thermal shutdown.	CPU, GM45, ICH9M
SMB_CK	I/O OD	CMOS	3.3V Sus.	3.3V	Act. PU	System Management Bus bidirectional clock line. Power sourced through 5V standby rail and main power rails.	ICH9M
SMB_DAT	I/O OD	CMOS	3.3V Sus.	3.3V	Act. PU	System Management Bus bidirectional data line. Power sourced through 5V standby rail and main power rails.	ICH9M
SMB_ALERT#	I	CMOS	3.3V Sus.	3.3V	10k PU	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. Power sourced through 5V standby rail and main power rails.	ICH9M

2.10.17 General Purpose I/O

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
GPO[0..3]	O	CMOS	3.3V	3.3V		General purpose output pins. Upon a hardware reset, these outputs are low.	ICH9M GPIOs [28, 08, 26, 10]
GPI[0:3]	I	CMOS	3.3V	3.3V	10k PU	General purpose input pins. Pulled high internally on the module.	ICH9M GPIOs [36, 37, 38, 39]

2.10.18 Module Type Definition

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
TYPE[0:2]#	Type Detect					The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) rare no-connects (NC). For Pin-out Type 1, these pins are don't care (X). TYPE2# TYPE1# TYPE0# X X X Pin-out Type 1 **NC NC NC Pin-out Type 2** NC NC GND Pin-out Type 3 (no IDE) NC GND NC Pin-out Type 4 (no PCI) NC GND GND Pin-out Type 5 (no IDE, no PCI) The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin- out type is detected. The Carrier Board logic may also implement a fault indicator such as a LED.	For this Type 2 board, all Type Detect pins are n.c.

2.10.19 Power and GND

Signal	Pin Type	Signal Level	Power Rail	Remark / Power Tol.	PU/PD	Description	Source / Target
VCC_12V	Power		12V (±5%)			Primary power input: +12V (±5%)	Voltage Regulators
VCC_5V_SBY	Power		5V (±5%)			Standby power input: +5.0V (±5%) If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	VCC3.3V SUS regulator
VCC_RTC	Power					Real-time clock circuit-power input : +3.0V (+2.0V to +3.3V)	ICH9M
GND	Power					Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	

2.11 Pin List for MSC CXB-GM45 module (Type 2)

Row A		Row B		Row C		Row D	
A1	GND (FIXED)	B1	GND (FIXED)	C1	GND (FIXED)	D1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#	C2	IDE_D7	D2	IDE_D5
A3	GBE0_MDI3+	B3	LPC_FRAME#	C3	IDE_D6	D3	IDE_D10
A4	GBE0_LINK100#	B4	LPC_AD0	C4	IDE_D3	D4	IDE_D11
A5	GBE0_LINK1000#	B5	LPC_AD1	C5	IDE_D15	D5	IDE_D12
A6	GBE0_MDI2-	B6	LPC_AD2	C6	IDE_D8	D6	IDE_D4
A7	GBE0_MDI2+	B7	LPC_AD3	C7	IDE_D9	D7	IDE_D0
A8	GBE0_LINK#	B8	LPC_DRQ0#	C8	IDE_D2	D8	IDE_REQ
A9	GBE0_MDI1-	B9	LPC_DRQ1#	C9	IDE_D13	D9	IDE_IOW#
A10	GBE0_MDI1+	B10	LPC_CLK	C10	IDE_D1	D10	IDE_ACK#
A11	GND (FIXED)	B11	GND (FIXED)	C11	GND (FIXED)	D11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#	C12	IDE_D14	D12	IDE_IRQ
A13	GBE0_MDI0+	B13	SMB_CK	C13	IDE_IORDY	D13	IDE_A0
A14	GBE0_CTREF	B14	SMB_DAT	C14	IDE_IOR#	D14	IDE_A1
A15	SUS_S3#	B15	SMB_ALERT#	C15	PCI_PME#	D15	IDE_A2
A16	SATA0_TX+	B16	SATA1_TX+	C16	PCI_GNT2#	D16	IDE_CS1#
A17	SATA0_TX-	B17	SATA1_TX-	C17	PCI_REQ2#	D17	IDE_CS3#
A18	SUS_S4#	B18	SUS_STAT#	C18	PCI_GNT1#	D18	IDE_RESET#
A19	SATA0_RX+	B19	SATA1_RX+	C19	PCI_REQ1#	D19	PCI_GNT3#
A20	SATA0_RX-	B20	SATA1_RX-	C20	PCI_GNT0#	D20	PCI_REQ3#
A21	GND (FIXED)	B21	GND (FIXED)	C21	GND (FIXED)	D21	GND (FIXED)
A22	SATA2_TX+	B22	SATA3_TX+	C22	PCI_REQ0#	D22	PCI_AD1
A23	SATA2_TX-	B23	SATA3_TX-	C23	PCI_RESET#	D23	PCI_AD3
A24	SUS_S5#	B24	PWR_OK	C24	PCI_AD0	D24	PCI_AD5
A25	SATA2_RX+	B25	SATA3_RX+	C25	PCI_AD2	D25	PCI_AD7
A26	SATA2_RX-	B26	SATA3_RX-	C26	PCI_AD4	D26	PCI_C/BE0#
A27	BATLOW#	B27	WDT	C27	PCI_AD6	D27	PCI_AD9
A28	ATA_ACT#	B28	AC_SDIN2	C28	PCI_AD8	D28	PCI_AD11
A29	AC_SYNC	B29	AC_SDIN1	C29	PCI_AD10	D29	PCI_AD13
A30	AC_RST#	B30	AC_SDIN0	C30	PCI_AD12	D30	PCI_AD15
A31	GND (FIXED)	B31	GND (FIXED)	C31	GND (FIXED)	D31	GND (FIXED)
A32	AC_BITCLK	B32	SPKR	C32	PCI_AD14	D32	PCI_PAR
A33	AC_SDOUT	B33	I2C_CK	C33	PCI_C/BE1#	D33	PCI_SERR#
A34	BIOS_DISABLE#	B34	I2C_DAT	C34	PCI_PERR#	D34	PCI_STOP#
A35	THRMTRIP#	B35	THRM#	C35	PCI_LOCK#	D35	PCI_TRDY#
A36	USB6-	B36	USB7-	C36	PCI_DEVSEL#	D36	PCI_FRAME#
A37	USB6+	B37	USB7+	C37	PCI_IRDY#	D37	PCI_AD16
A38	USB_6_7_OC#	B38	USB_4_5_OC#	C38	PCI_C/BE2#	D38	PCI_AD18
A39	USB4-	B39	USB5-	C39	PCI_AD17	D39	PCI_AD20
A40	USB4+	B40	USB5+	C40	PCI_AD19	D40	PCI_AD22
A41	GND (FIXED)	B41	GND (FIXED)	C41	GND (FIXED)	D41	GND (FIXED)
A42	USB2-	B42	USB3-	C42	PCI_AD21	D42	PCI_AD24
A43	USB2+	B43	USB3+	C43	PCI_AD23	D43	PCI_AD26
A44	USB_2_3_OC#	B44	USB_0_1_OC#	C44	PCI_C/BE3#	D44	PCI_AD28
A45	USB0-	B45	USB1-	C45	PCI_AD25	D45	PCI_AD30
A46	USB0+	B46	USB1+	C46	PCI_AD27	D46	PCI_IRQC#
A47	VCC_RTC	B47	EXCD1_PERST#	C47	PCI_AD29	D47	PCI_IRQD#
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	C48	PCI_AD31	D48	PCI_CLKRUN#
A49	EXCD0_CPPE#	B49	SYS_RESET#	C49	PCI_IRQA#	D49	*n.c. (PCI_M66EN)*
A50	LPC_SERIRQ	B50	CB_RESET#	C50	PCI_IRQB#	D50	PCI_CLK

	= not supported on MSC CXB-GM45 module

Row A		Row B		Row C		Row D	
A51	GND (FIXED)	B51	GND (FIXED)	C51	GND (FIXED)	D51	GND (FIXED)
A52	*n.c. (PCIE_TX5+)*	B52	*n.c. PCIE_RX5+*	C52	PEG_RX0+	D52	PEG_TX0+
A53	*n.c. (PCIE_TX5-)*	B53	*n.c. PCIE_RX5-*	C53	PEG_RX0-	D53	PEG_TX0-
A54	GPI0	B54	GPO1	C54	TYPE0#	D54	PEG_LANE_RV#
A55	PCIE_TX4+	B55	PCIE_RX4+	C55	PEG_RX1+	D55	PEG_TX1+
A56	PCIE_TX4-	B56	PCIE_RX4-	C56	PEG_RX1-	D56	PEG_TX1-
A57	GND	B57	GPO2	C57	TYPE1#	D57	TYPE2#
A58	PCIE_TX3+	B58	PCIE_RX3+	C58	PEG_RX2+	D58	PEG_TX2+
A59	PCIE_TX3-	B59	PCIE_RX3-	C59	PEG_RX2-	D59	PEG_TX2-
A60	GND (FIXED)	B60	GND (FIXED)	C60	GND (FIXED)	D60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+	C61	PEG_RX3+	D61	PEG_TX3+
A62	PCIE_TX2-	B62	PCIE_RX2-	C62	PEG_RX3-	D62	PEG_TX3-
A63	GPI1	B63	GPO3	C63	RSVD	D63	RSVD
A64	PCIE_TX1+	B64	PCIE_RX1+	C64	RSVD	D64	RSVD
A65	PCIE_TX1-	B65	PCIE_RX1-	C65	PEG_RX4+	D65	PEG_TX4+
A66	GND	B66	WAKE0#	C66	PEG_RX4-	D66	PEG_TX4-
A67	GPI2	B67	WAKE1#	C67	RSVD	D67	GND
A68	PCIE_TX0+	B68	PCIE_RX0+	C68	PEG_RX5+	D68	PEG_TX5+
A69	PCIE_TX0-	B69	PCIE_RX0-	C69	PEG_RX5-	D69	PEG_TX5-
A70	GND (FIXED)	B70	GND (FIXED)	C70	GND (FIXED)	D70	GND (FIXED)
A71	LVDS_A0+	B71	LVDS_B0+	C71	PEG_RX6+	D71	PEG_TX6+
A72	LVDS_A0-	B72	LVDS_B0-	C72	PEG_RX6-	D72	PEG_TX6-
A73	LVDS_A1+	B73	LVDS_B1+	C73	SDVO_DATA	D73	SDVO_CLK
A74	LVDS_A1-	B74	LVDS_B1-	C74	PEG_RX7+	D74	PEG_TX7+
A75	LVDS_A2+	B75	LVDS_B2+	C75	PEG_RX7-	D75	PEG_TX7-
A76	LVDS_A2-	B76	LVDS_B2-	C76	GND	D76	GND
A77	LVDS_VDD_EN	B77	LVDS_B3+	C77	RSVD	D77	IDE_CBLID#
A78	LVDS_A3+	B78	LVDS_B3-	C78	PEG_RX8+	D78	PEG_TX8+
A79	LVDS_A3-	B79	LVDS_BKLT_EN	C79	PEG_RX8-	D79	PEG_TX8-
A80	GND (FIXED)	B80	GND (FIXED)	C80	GND (FIXED)	D80	GND (FIXED)
A81	LVDS_A_CK+	B81	LVDS_B_CK+	C81	PEG_RX9+	D81	PEG_TX9+
A82	LVDS_A_CK-	B82	LVDS_B_CK-	C82	PEG_RX9-	D82	PEG_TX9-
A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL	C83	RSVD	D83	RSVD
A84	LVDS_I2C_DAT	B84	VCC_5V_SBY	C84	GND	D84	GND
A85	GPI3	B85	VCC_5V_SBY	C85	PEG_RX10+	D85	PEG_TX10+
A86	KBD_RST#	B86	VCC_5V_SBY	C86	PEG_RX10-	D86	PEG_TX10-
A87	KBD_A20GATE	B87	VCC_5V_SBY	C87	GND	D87	GND
A88	PCIE0_CK_REF+	B88	RSVD	C88	PEG_RX11+	D88	PEG_TX11+
A89	PCIE0_CK_REF-	B89	VGA_RED	C89	PEG_RX11-	D89	PEG_TX11-
A90	GND (FIXED)	B90	GND (FIXED)	C90	GND (FIXED)	D90	GND (FIXED)
A91	RSVD	B91	VGA_GRN	C91	PEG_RX12+	D91	PEG_TX12+
A92	RSVD	B92	VGA_BLU	C92	PEG_RX12-	D92	PEG_TX12-
A93	GPO0	B93	VGA_HSYNC	C93	GND	D93	GND
A94	RSVD	B94	VGA_VSYNC	C94	PEG_RX13+	D94	PEG_TX13+
A95	RSVD	B95	VGA_I2C_CK	C95	PEG_RX13-	D95	PEG_TX13-
A96	GND	B96	VGA_I2C_DAT	C96	GND	D96	GND
A97	VCC_12V	B97	*n.c. (TV_DAC_A)*	C97	RSVD	D97	PEG_ENABLE#
A98	VCC_12V	B98	*n.c. (TV_DAC_B)*	C98	PEG_RX14+	D98	PEG_TX14+
A99	VCC_12V	B99	*n.c. (TV_DAC_C)*	C99	PEG_RX14-	D99	PEG_TX14-
A100	GND (FIXED)	B100	GND (FIXED)	C100	GND (FIXED)	D100	GND (FIXED)
A101	VCC_12V	B101	VCC_12V	C101	PEG_RX15+	D101	PEG_TX15+
A102	VCC_12V	B102	VCC_12V	C102	PEG_RX15-	D102	PEG_TX15-
A103	VCC_12V	B103	VCC_12V	C103	GND	D103	GND
A104	VCC_12V	B104	VCC_12V	C104	VCC_12V	D104	VCC_12V
A105	VCC_12V	B105	VCC_12V	C105	VCC_12V	D105	VCC_12V
A106	VCC_12V	B106	VCC_12V	C106	VCC_12V	D106	VCC_12V
A107	VCC_12V	B107	VCC_12V	C107	VCC_12V	D107	VCC_12V
A108	VCC_12V	B108	VCC_12V	C108	VCC_12V	D108	VCC_12V

Row A		Row B		Row C		Row D	
A109	VCC_12V	B109	VCC_12V	C109	VCC_12V	D109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)	C110	GND (FIXED)	D110	GND (FIXED)

	= not supported on MSC CXB-GM45 module

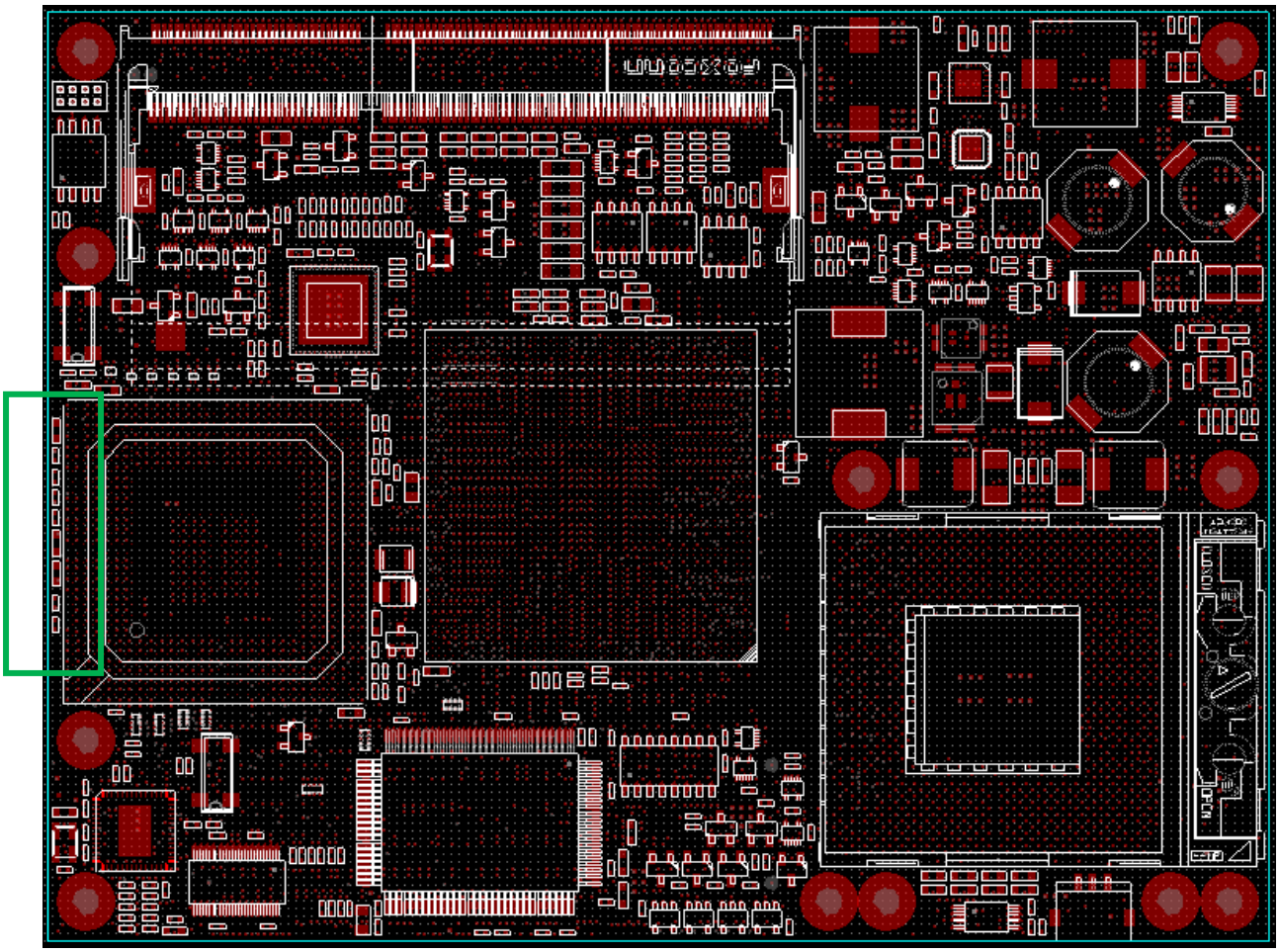
3 Jumpers and Connectors

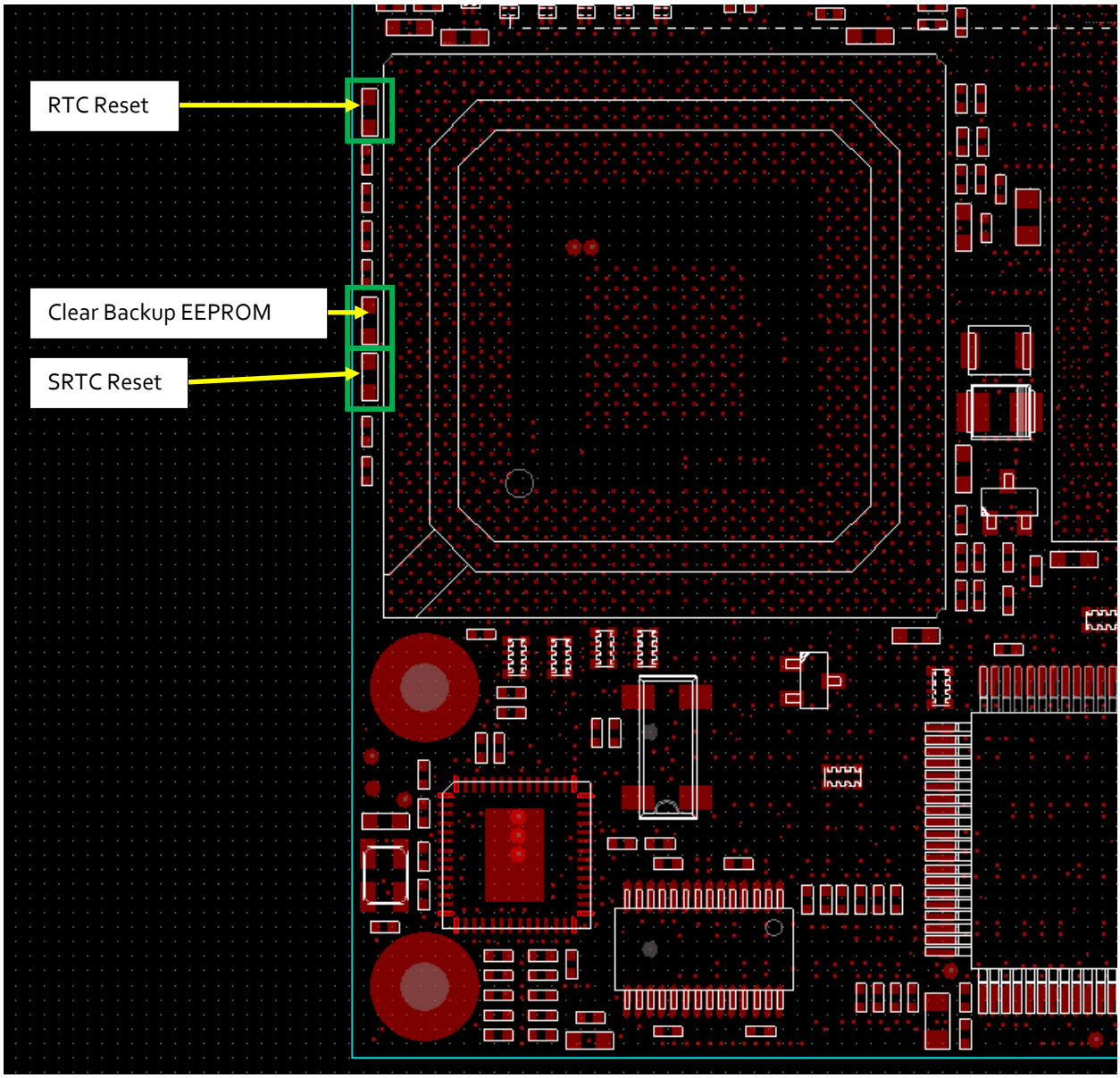
3.1 Jumpers

There are three jumpers available on the module:

- RTC Reset: By shorting the pins of this jumper, the RTC Clock is reset and the values of the CMOS NV-RAM are cleared
- SRTC Reset: By shorting the pins of this jumper, the manageability register bits in the CMOS NV-RAM are reset
- Clear Backup EEPROM: By shorting the pins of this jumper, the values of the Backup EEPROM and the values of the NV-ROM are invalidated, thus forcing the board to start up with default values.

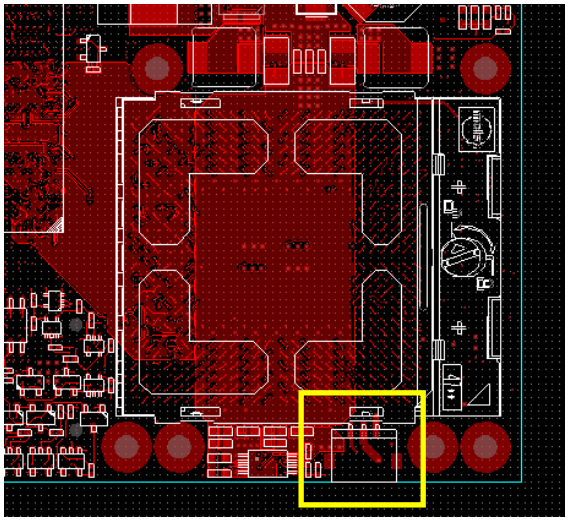
These jumpers are located at the top side of the board at the border, beneath the ICH9M south bridge:

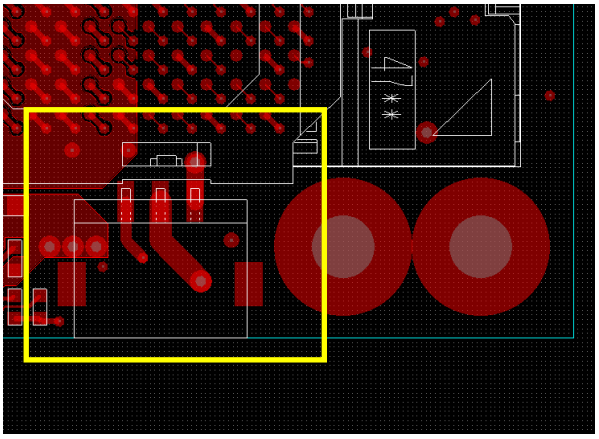




3.2 Fan Connector

The connector of the fan is located at top side of the CPU module, directly beneath the CPU socket:





The following connector types are used:

- JST S3B-ZR-SM3A-TF
- JST S3B-ZR-SM4A-TF(LF)
- Würth Elektronik 648103131822

The fan itself should be equipped with a JST ZHR-3 Connector. The pinning is as following (numbering from right to left):

Pin	Signal	Description
1	GND	GND
2	PWM	Output of the PWM-Signal to drive the fan, amplitude max. 12V
3	Tacho	Input for the tacho signal of the fan (O.C.)

4 Watchdog

The CXB-GM45 board has a watchdog function implemented in a PIC Microcontroller.

The watchdog can be enabled and configured in the BIOS Setup.

If the watchdog is enabled a counter is started which generates a reset if it is not retriggered within a programmable time window.

Possible watchdog delays: 1s, 5s, 10s, 30s, 1min, 5min, 10min, 30min Possible watchdog timeout: 0.4s, 1s, 5s, 10s, 30s, 1min, 5min, 10min The time delay starts as soon as it is enabled in the BIOS.

MSC provides a software API which gives the application software access to the Watchdog functionality if needed.

5 System resources

5.1 PCI IRQ Routing

			Interrupts of Controller (ICH-9M)							
Slot Number (or Onboard Device)	IDSEL # or DEV. #	Bus #	PIRQ 0 (INT A)	PIRQ 1 (INT B)	PIRQ 2 (INT C)	PIRQ 3 (INT D)	PIRQ 4 (INT E)	PIRQ 5 (INT F)	PIRQ 6 (INT G)	PIRQ 7 (INT H)
PCIe x16 Root Port	Dev 1 Fn 0	0	A							
Internal Graphic	Dev 2 Fn 0	0	A							
AMT Controller	Dev 3 Fn 0	0	A							
MEI (if enabled)	Dev 3 Fn 1	0				D				
IDER (if enabled)	Dev 3 Fn 2	0			C					
SOL (if enabled)	Dev 3 Fn 3	0		B						
GBit LAN Controller	Dev 25 Fn 0	0					A			
UHCI (USB1.1) Host										
USB Ports 0,1	Dev 29 Fn 0	0								A
USB Ports 2,3	Dev 29 Fn 1	0				B				
USB Ports 4,5	Dev 29 Fn 2	0			C					
USB Ports 6,7	Dev 26 Fn 0	0	A							
EHCI (USB2.0) Host										
USB Ports 0-5	Dev 29 Fn 7	0								A
USB Ports 6-7	Dev 26 Fn 7	0				C				
HD Audio	Dev 27 Fn 0	0							A	
PCIe x1 Root Port										
for Slot 1	Dev 28 Fn 0	0		A						
for Slot 2	Dev 28 Fn 1	0	B							
for Slot 3	Dev 28 Fn 2	0			C					
for Slot 4	Dev 28 Fn 3	0				D				
for Slot 5	Dev 28 Fn 4	0		A						
SATA Controller 1	Dev 31 Fn 2	0				B				
SATA Controller 2	Dev 31 Fn 5	0				B				
SMBus Controller	Dev 31 Fn 3	0				C				
PCIe x16 Slot	Dev 0 Fn 0	1	A	B	C	D				
PCIe x1 Slot 1	Dev 0 Fn 0	dyn	A	B	C	D				
PCIe x1 Slot 2	Dev 0 Fn 0	dyn	D	A	B	C				
PCIe x1 Slot 3	Dev 0 Fn 0	dyn	C	D	A	B				
PCIe x1 Slot 4	Dev 0 Fn 0	dyn	B	C	D	A				
PCIe x1 Slot 5	Dev 0 Fn 0	dyn	A	B	C	D				
PCI Slot 1	AD20 / Dev 4	dyn					A	B	C	D
PCI Slot 2	AD21 / Dev 5	dyn					D	A	B	C
PCI Slot 3	AD22 / Dev 6	dyn					C	D	A	B
PCI Slot 4	AD23 / Dev 7	dyn					B	C	D	A
PATA Controller	Dev 8 Fn 0	dyn			A					

5.2 Carrier Board PCI Resource Allocation

The external PCI resource allocation on the carrier board should be as follows:

Slot / Device Signal	Slot / Device 0	Slot / Device 1	Slot / Device 2	Slot / Device 3
IDSEL	PCI_AD[20]	PCI_AD[21]	PCI_AD[22]	PCI_AD[23]
PCI Clock	PCI_CLK replica	PCI_CLK replica	PCI_CLK replica	PCI_CLK replica
INTA#	PCI_IRQ[A]#	PCI_IRQ[B]#	PCI_IRQ[C]#	PCI_IRQ[D]#
INTB# (if used)	PCI_IRQ[B]#	PCI_IRQ[C]#	PCI_IRQ[D]#	PCI_IRQ[A]#
INTC# (if used)	PCI_IRQ[C]#	PCI_IRQ[D]#	PCI_IRQ[A]#	PCI_IRQ[B]#
INTD# (if used)	PCI_IRQ[D]#	PCI_IRQ[A]#	PCI_IRQ[B]#	PCI_IRQ[C]#
REQ0# (if used)	PCI_REQ[0]#	PCI_REQ[1]#	PCI_REQ[2]#	PCI_REQ[3]#
REQ1# (if used)	PCI_REQ[1]#	PCI_REQ[2]#	PCI_REQ[3]#	PCI_REQ[0]#
REQ2# (if used)	PCI_REQ[2]#	PCI_REQ[3]#	PCI_REQ[0]#	PCI_REQ[1]#
REQ3# (if used)	PCI_REQ[3]#	PCI_REQ[0]#	PCI_REQ[1]#	PCI_REQ[2]#
GNT0# (if used)	PCI_GNT[0]#	PCI_GNT[1]#	PCI_GNT[2]#	PCI_GNT[3]#
GNT1# (if used)	PCI_GNT[1]#	PCI_GNT[2]#	PCI_GNT[3]#	PCI_GNT[0]#
GNT2# (if used)	PCI_GNT[2]#	PCI_GNT[3]#	PCI_GNT[0]#	PCI_GNT[1]#
GNT3# (if used)	PCI_GNT[3]#	PCI_GNT[0]#	PCI_GNT[1]#	PCI_GNT[2]#

The signals PCI_IRQx, PCI_REQx or PCI_GNTx are are routed exclusively to the COM Express connector. They are not shared on the CPU board.

5.3 SMB Address Map

Device	A6	A5	A4	A3	A2	A1	A0	R/W	address *)
SMBus host (ICH9-M slave)	0	0	0	1	0	0	0	x	10h / 08h
SMSC EMC2104	0	1	0	1	1	1	1	x	5Eh / 2Fh
ICS9LPRS365 Clock Synthesizer	1	1	0	1	0	0	1	x	D2h / 69h
CMOS backup EEPROM	1	0	1	0	1	0	0	x	A8h / 54h AAh / 55h
SPD EEPROM (SO-DIMM)	1	0	1	0	0	0	0	x	A0h / 50h A2h / 51h

*) 8 bit address (with R/W) / 7 bit address (without R/W)

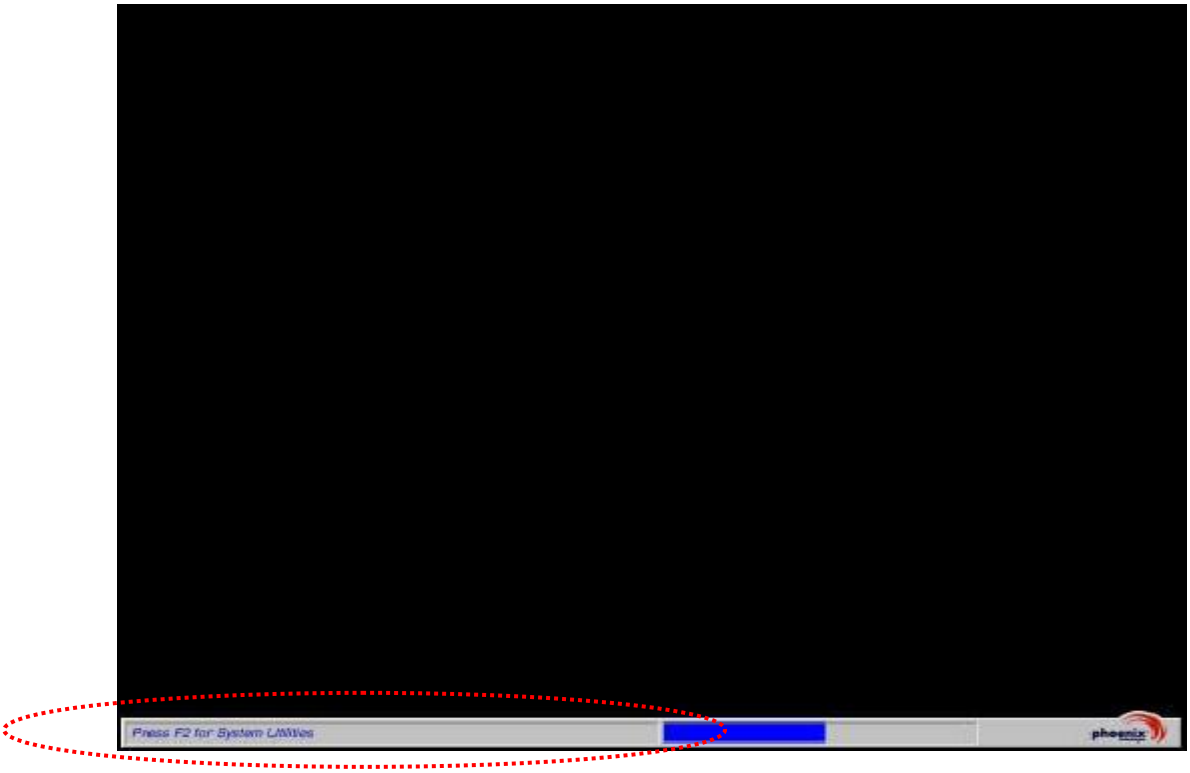
6 BIOS

6.1 Introduction

This guide describes the Phoenix SecureCore Startup screen and contains information on how to access Phoenix SecureCore setup to modify the settings which control Phoenix pre-OS (operating system) functions.

6.1.1 Startup Screen Overview

The Phoenix SecureCore Startup screen is a graphical user interface (GUI) that is included in Phoenix SecureCore products. The default bios behavior is to show an informational text screen during bios POST phase, but the graphical boot screen can be enabled in the bios setup. The standard boot screen is a black screen, including a progress bar at the bottom of the screen. This bar indicates the progress of the Startup Screen functions and provides user prompting and POST status. The following figure shows the various parts of a generic Startup Screen at 1024x768 resolution:



6.1.2 Activity Detection Background

While the Startup screen is displayed, press the Setup Entry key (F2 – SecureCore default). The SecureCore Startup Status Bar acknowledges the input, and at the end of POST, the screen clears and setup launches.

An example of the Startup Status Bar displaying changing state is shown in the following figure. The "Please Wait..." text is displayed after the F2 key is pressed to acknowledge user input.

Active status bar:

6.2 SecureCore Setup Utility

With the Phoenix SecureCore Setup program, you can modify SecureCore settings and control the special features of your computer. The Setup program uses a number of menus for making changes and turning the special features on or off. This chapter provides an overview of the Setup utility and describes at a high-level how to use it.

6.2.1 Configuring the System BIOS

To start the Phoenix SecureCore Setup utility, press [F2] to launch Setup. The Setup main menu appears.

6.2.2 The BIOS Menu Structure

The BIOS Menu is structured in the following way:

Main		
	Board Information	
	SATA Port 1	
	SATA Port 2	
	SATA Port 3	
	SATA Port 4	
	PATA Master	
	PATA Slave	
	Keyboard Features	
	Boot Options	
Advanced		
	CPU Control Sub-Menu	
	MCH Control Sub-Menu	
	Video (Intel IGD) Control Sub-Menu	
	ICH Control Sub-Menu	
		PCI Express Control Sub-Menu
		PCI Control Sub-Menu
		ICH USB Control Sub-Menu
	ACPI Control Sub-Menu	
	I/O Device Configuration	
	Watchdog Options	
	AMT Sub-Menu	
Security		
Power		
	Hardware Monitor	
Boot		
Exit		

The Menu Bar

The Menu Bar at the top of the window lists these selections:

Menu Items	Description
Main	Use this menu for basic system configuration.
Advanced	Use this menu to set the Advanced Features available on your system's chipset.
Security	Use this menu to set User and Supervisor Passwords and the Backup and Virus-Check reminders.
Power	Use this menu to configure Power-Management features.
Boot	Use this menu to set the boot order in which the BIOS attempts to boot to OS.
Exit	Exits the current menu.

Use the left and right arrow keys on your keyboard to make a menu selection.

The Legend Bar

Use the keys listed in the legend bar on the bottom of the screen to make your selections, or to exit the current menu. The following table describes the legend keys and their alternates:

Key	Function
F1 or Alt-H	General Help window.
Esc	Exit this menu.
Arrow keys	Select a different menu.
Up and down arrow keys	Move cursor up and down.
Tab or Shift-Tab	Move cursor left and right (i.e. at System Time / System Date).
Home or End	Move cursor to top or bottom of window.
PgUp or PgDn	Move cursor to next or previous page.
F5 or -	Select the previous value for the field.
F6 or + or Space	Select the next value for the field.
F9	Load the Default Configuration values (for all menus).
F10	Save and exit.
Enter	Execute command or select submenu.

Select an item

To select an item, use the arrow keys to move the cursor to the field you want. Then use the plus-and-minus value keys to select a value for that field. The Save Values commands in the Exit Menu save the values currently displayed in all the menus.

Display a submenu

To display a submenu, use the arrow keys to move the cursor to the sub menu you want. Then press Enter. A pointer marks all submenus.

6.2.3 The Main Menu

You can make the following selections on the Main Menu itself. Use the sub menus for other selections.

Feature	Options	Description
Board Information	Submenu	Displays BIOS Version
System Time	Enter Time (HH:MM:SS)	Set the System Time.
System Date	Enter Date (DD/MM/YYYY)	Set the System Date.
SATA Port 1	Submenu “Master & Slaves”	Configure SATA Port 1
SATA Port 2	Submenu “Master & Slaves”	Configure SATA Port 2
SATA Port 3	Submenu “Master & Slaves”	Configure SATA Port 3
SATA Port 4	Submenu “Master & Slaves”	Configure SATA Port 4
PATA Master	Submenu “Master & Slaves”	Configure IDE Channel 0 Master
PATA Slave	Submenu “Master & Slaves”	Configure IDE Channel 0 Slave
Keyboard Features	Submenu	Configure Keyboard Features
Boot Options	Submenu	Configure Boot Options

6.2.3.1 Board Information

Feature	Options	Description
HW Platform	Informative	Name of the hardware platform
HW Revision	Informative	Hardware revision number
Bios Version	Informative	Shows current bios version.
Serial #	Informative	Hardware Serial Number
Boot Counter	Informative	The number of times this board has booted up.
CPU String	Informative	CPU Identification string
CPU Speed	Informative	CPU Speed
CPU Class	Informative	CPU ID Class code
CPU Model	Informative	CPU ID Model code
CPU Stepping	Informative	CPU ID Stepping
CPU Cores	Informative	Number of CPU cores
MicroCode Patch ID	Informative	Patch ID of the Microcode
Northbridge	Informative	Identification of the northbridge
Southbridge	Informative	Identification of the southbridge
System Memory	Informative	Amount of memory below 1MB
Extended Memory	Informative	Total amount of memory

6.2.3.2 Masters & Slaves

The **Master** and **Slave** settings on the Main Menu control these types of devices:

- **Hard-disk drives (IDE and SATA)**
- **Removable-disk drives**
- **CD-ROM drives**

There is one IDE connector on your motherboard, usually labeled "Primary IDE". There are usually two connectors on each ribbon cable attached to IDE connector. When you have connected two drives to this connector, the one on the end of the cable is the Master.

When you enter Setup, the Main Menu displays the results of **Autotyping** information each drive provides about its own size and other characteristics–and how they are arranged as Masters or Slaves on your machine.

Note: Do not attempt to change these settings unless you have an installed drive that does not autotype properly (such as an older hard-disk drive that does not support autotyping).

If you need to change your drive settings, select one of the Master or Slave drives on the Main Menu. This will display a menu like this:

Note: The capacity is displayed in 'real' Mbytes (1MB=1024*1024 Bytes) Drives with a total capacity greater than 8Gbyte operate in LBA format only.

Feature	Options	Description
Type	None, Auto, User, ATAPI Removable, Other ATAPI, CD-ROM	**None** = Autotyping is not able to supply the drive type or end user has selected None, disabling any drive that may be installed. **Auto** = Autotyping, the drive itself supplies the information. **User** = You supply the hard-disk drive information in the following fields. **ATAPI Removable** = Removable Disk Drive **Other ATAPI** = non-specific ATAPI Device **CD-ROM** = CD-ROM drive.
Cylinders	1 to 65536	Number of Cylinders
Heads	1 to 16	Number of read/write heads
Sectors	1 to 63	Number of sectors per track
Multi-Sector Transfers	Disabled, 2 sectors, 4 sectors, 8 sectors, 16 sectors	Any selection except **Disabled** determines the number of sectors transferred per block.
LBA Mode Control	Disabled, Enabled	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads, & Sectors.
32 Bit I/O	Disabled, Enabled	Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus.
Transfer Mode	Standard Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO 3 / DMA 1 FPIO 4 / DMA 2	Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.
Ultra DMA Mode	Disabled Mode 0 Mode 1 Mode 2 Mode 3 Mode 4 Mode 5 Mode 6	Ultra DMA Mode supports 33/66/100 MB/sec transfer rate for fixed disk drives.

Feature	Options	Description
SMART Monitoring	Disabled, Enabled	Displays the status of SMART Monitoring if supported by the used drive.

WARNING: Incorrect settings can cause your system to malfunction.

6.2.3.3 Keyboard Features

Feature	Options	Description
NumLock	On, Off, Auto	Selects Power-on state for NumLock
Key Click	Disabled, Enabled	Enables key click
Keyboard auto-repeat	30/sec 26.7/sec 21.8/sec 18.5/sec 13.3/sec 10/sec 6/sec 2/sec	Selects key repeat rate
Keyboard auto-repeat rate	0.25s, 0.5s, 0.75s, 1s	Selects delay before key repeat

6.2.3.4 Boot Options

Feature	Options	Description
Summary screen	Disabled, Enabled	**Enabled** displays system configuration on boot.
Boot-time Diagnostic Screen	Disabled, Enabled	**Enabled** displays the diagnostic screen during boot. **Disabled** displays the Boot Logo.
Quick Boot Mode	Disabled, Enabled	**Enabled** allows POST to skip certain test while booting. This will decrease the time needed to boot the system.
POST Errors	Disabled, Enabled	Pauses and displays Setup entry or resume boot prompt if error occurs on boot. If disabled, system always attempts to boot
Legacy OS Boot	Disabled, Enabled	Select Enabled to attempt Legacy OS Boot only. Select Disabled to attempt EFI Boot first, Legacy OS second.

6.2.4 The Advanced Menu

Feature	Options	Description
Installed O/S	Other, Win95, Win98, WinMe, Win2000, WinXP	Select the operating system installed on your system which you will use most commonly. **NOTE**: An incorrect setting can cause some operating systems to display unexpected behavior.
Reset configuration Data	No, Yes	Select 'Yes' if you want to clear the Extended System Configuration Data (ESCD) area.
Large Disk Access Mode	Other, DOS	Select **Other** for UNIX, Novell NetWare. Select **DOS** for all other operating systems.
Small Disk Access Mode	No, Yes	Select if CHS translation should be made for a LBA-capable harddisk with less than 1024 cylinders, e.g. CompactFlash(R). If you have problems with booting from a CompactFlash(R), try to change this setting. No = translate CHS only if HDD has >1024 cyls. Yes = translate CHS for all LBA-capable disks.
Port 80 Cycles	LPC Bus, PCI Bus	Control where the Port 80h cycles are sent.
Video Repost	Disabled, Linux, Enabled	Select If a Video Repost is to be performed during resume from S3. Disabled: Never perform a Video Repost upon resome from S3. Linux: Only perform a Video Repost IF the OS is Linux. Enabled: Always perform a Video Repost upon resume from S3.
CPU Control Sub-Menu	Sub-Menu	Configure Yonah / Merom CPU Control
MCH Control Sub-Menu	Sub-Menu	Configure MCH Control
Video (Intel IGD) Control Sub-Menu	Sub-Menu	Configure Video (Intel IGD) Control
ICH Control Sub-Menu	Sub-Menu	Configure ICH Control
ACPI Control Sub-Menu	Sub-Menu	Configure ACPI Control
I/O Device Configuration	Sub-Menu	Configure I/O Device

Feature	Options	Description
Watchdog Options	Sub-Menu	Configure Watchdog Options
AMT Sub-Menu	Sub-Menu	Configure AMT Options

6.2.4.1 CPU Control Sub-Menu

Note: Depending on the CPU type you are using, some options of the CPU Control Sub-Menu can be hidden in consequence of different CPU type features that exist.

Feature	Options	Description
VTD Feature	Disabled, Enabled	VT-d supports the remapping of I/O DMA transfers and device-generated interrupts in a VM. Note: Vt-d must be supported by the Virtual Machine Manager.
Core Multi Processing	Disabled, Enabled	Determines whether the 2nd core is enabled. Disabled = 2nd core is disabled Enabled = 2nd core is enabled
Intel ® SpeedStep™	Disabled, Enabled	Allows more than two frequency range to be supported Note: Intel ® Celeron CPU's do not support Intel ® SpeedStep™.
CX States	Disabled, Enabled	Enable CPU C-States: Main switch for C0, C1, C2, C3, C4, Deep C4, C6
Enhanced C-States Enable	Disabled, Enabled	Enables Enhanced C-State support. Disabled = Enhanced C-States disabled. Enabled = Enhanced C-State enable.
Deep C4	Disabled, Enabled	Intel® Enhanced Deeper Sleep Enable bit
Hard C4	Disabled, Enabled	Set this bit enable the Package C4/Deep C4 exit VID's to min of EIST operating point upon #DPRSLP

Feature	Options	Description
C6	Disabled, Enabled	Enable deep power down technology state.
No Execute Mode MemProtection	Disbaled, Enabled	Prevents attacks again system
Intel® Virtualization Technology	Disabled, Enabled	When enabled, a VMM utilize the additional hardware virtualization capabilities provided by this technology
T States	Disabled, Enabled	Enables Processor throttling states
Thermal Control Circuit	Disabled, TM1, TM2, TM1 and TM2	Setting this bit enables the thermal control circuit (TCC) portion of the Thermal Monitor feature of the CPU. TM1 = 50% duty Cycle TM2 = Geyserville III
PROCHOT# Enable	Disabled, Enabled	Enables the processors's PROCHOT# signal. If asserted, the TMx circuit will be engaged. PROCHOT# is in addition to the TCC and Enhanced TCC circuitry inside the processor, and either may engage TMx.

6.2.4.2 MCH Control Sub-Menu

Feature	Options	Description
PCI Express Graphics Size	256 MB, 128 MB, 64 MB	Selects variable size PCI-Express config space.
Dynamic FSB	Disabled, Enabled	Enable/Disable dynamic FSB.
Option for System memory Frequency	Disabled, Enabled	Disable: No change in System memory frequency Enable: System memory setting as 667MHz
DMI Link ASPM Support	Enabled, Disabled	Enable/disable the control of Active State Power Management on both GMCH side and ICH9 side of the DMI Link.
Stop Grant Configuration	Auto, Manual	Automatic/Manual stop grant configuration.
Number of Stop Grant cycles	0-63	Selects number of Stop-Grant cycles

Feature	Options	Description
Always enable PEG	Disabled, Enabled	To enable PEG.
Force X1	Disabled, Enabled	Limits the width to X1.
PEG Port ASPM Support	Auto, Disabled	Control ASPM for the PEG Device Auto= will set APMC to the highest common supported ASPM between the Port and Endpoint.
Extended Synch	Disabled, Enabled	Enable PCIe Extended Synchronization for Logic analyser use.
MDA Support	Disabled, Enabled	Control MDA support for the PEG Device.

6.2.4.3 Video (Intel IGD) Control Sub-Menu

Feature	Options	Description
Default Primary Video Adapter	PEG, IGD	Select PEG to have PCI Express Graphics. If supported and enabled, be used for the boot display device. If selected and no PEG card is found, Internal Graphics will be used automatically. Select IGD to have Internal Graphics. If supported and enabled, be used for the boot display device. Select also to use PCI video.
IGD – Device 2	Disabled, Auto	Enables or Disable the Internal Graphics Device by setting item to the desired value.
IGD – Boot Type	VBIOS default, CRT, LFP, EFP, EFP2, CRT+LFP, CRT+EFP, CRT+EFP2	Select the Video Device that will be activated during POST.

Feature	Options	Description
IGD – LCD Panel Type	640x480, sp, 18bit 800x600, sp, 18bit 1024x768, sp, 18bit 1280x1024, dp, 18bit 1440x900, dp, 24bit 1400x1050, dp, 24 bit 1600x1200, dp, 24 bit 1280x1024, dp, 24 bit 1024x768, sp, 24bit 1920x1200, dp, 24bit 800x480, sp, 18bit 1280x800, sp, 18bit 1366x768, sp, 24bit 1440x900, dp, 18bit 1680x1050, dp, 24bit 1920x1080, dp, 24bit	Select the LCD panel used by the Internal Graphics Device by selecting the appropriate setup item. The first item is Panel 1, the last item is Panel 16. Some Panels are not numbered due to size constraints.
IGD – Panel Scaling	Auto, Force Scaling, Off, Maintain Aspect Ratio	Selects the LCD panel scaling option used by the Internal Graphics Device. 1. Auto 2. Force Scaling 3. Off
IGD – Backlight Brightness	10%, 20%, 30%, 40%, 50%, 60%, 70%, 80%, 90%, 100%	Select the starting brightness for the LVDS backlight signal. **Note**: Depending on the used backlight inverter it is possible that brightness scale could be inverted.
HDCP Mode	Disabled, Enabled	Enable/disable HDCP feature.
DVMT Pre-Allocated	32 MB, 64 MB, 128 MB	Select DVMT Pre Allocated (Fixed) Graphics Memory size used by the internal Graphics Device.
Total graphics Memory	128 MB, 256 MB, MaxDVMT	Select the amount of Total Graphics Memory Pre-Allocated + Fixed + DVMT for use by the Internal for use by the Internal Graphics Device.
PAVP Mode	Disabled, Lite, High	GMCH Protected Audio Video Path
Onboard EDID Eeprom	Disabled, Enabled	Enables or disables the Onboard EEPROM for EDID on LFP1.

6.2.4.4 ICH Control Sub-Menu

Feature	Options	Description
PCI Express Control Submenu	Sub-Menu	Configure PCI Express Control
PCI Control Submenu	Sub-Menu	Configure PCI Control
ICH USB Contol Submenu	Sub-Menu	Configure ICH USB Control
SATA Mode Selection	IDE, AHCI, Raid	Determines how SATA Controllers operate. IDE: Sata operates in IDE Mode AHCI: Sata operates in AHCI Mode Raid: Sata operates in Raid Mode **Note**: to configure Raid press CTRL-I after Post to enter Raid option Rom or install the Intel Matrix Storage Manager for XP/Vista. **Note**: Only 3 of 4 Sata Ports can be used for Raid. **Note**: To install XP in AHCI or Raid Mode, it is necessary to install ICH9M AHCI/Raid Driver during installation process. For XP a USB Floppy is needed to include drivers by pressing F6
Azalia – Device 27, Function 0	Disabled, Enabled, Auto	Control Detection of the Azalia Device. Disabled = Azalia will be unconditionally disabled, regardless of presence. Auto = Azalia will be enabled if present, disabled otherwise. Enabled = Azalia will be unconditionally enabled, regardless of presence (for Docking)
Azalia Modem PME Enable	Disabled, Enabled	Control the ability to wake the system from an Azalia Modem Device.
On–board LAN	Disabled, Enabled	Setting item to “Disabled” will remove the LAN from PCI Config Space. Setting item to “Enabled” will allow the LAN to operate correctly.
PXE OPROM	Disabled, Enabled	Enable PXE Option ROM.

Feature	Options	Description
PCI Clock Run	Disabled, Enabled	If enabled, the CLKRUN# logic will stop the PCI Clocks
Pop Up Mode Enable	Disabled, Enabled	Select the proper mode: If disabled, bus master traffic is a break event and it will return from C3/C4 to C0 based on break events. If enabled, ICH will observe a bus master request and it will take the system from a C3/C4 state to a C2 state and auto enable bus masters.
Pop Down Mode Enable	Disabled, Enabled	Should be enabled only if Pop up is enabled: If disabled, ICH will NOT attempt to automatically return. If enabled, ICH will observe a NO bus master request and it can return to a previous C3 or C4 state.

6.2.4.4.1 PCI Express Control Sub-Menu

Feature	Options	Description
PCI Express – Root Port 1-5	Disabled, Enabled, Auto	Control PCI Express Port via this setup option. Disabled = Port always Disabled. Auto = Only enable if card found. Note that if Root Port 1 is disabled Root Ports 2-5 will be disabled as well.
ASPM	Disabled, Enabled	Enable PCI Express Active State Power Management settings.
Automatic ASPM	Manual, auto	Automatically enable ASPM based on reported capabilities and know issue. **Note**: Only selectable if ASPM=enabled
ASPM L0s:	Disabled, Root Port Only Endpoint Port Only Both Root and Endpoint Ports	Enable PCIe ASPM L0s. **Note**: Only selectable if Automatic ASPM = manual.
ASPM L1	Disable, Enable	Enable PCIe L1. **Note**: Only selectable if Automatic ASPM = manual.

6.2.4.4.2 PCI Control Sub-Menu

Feature	Options	Description
PCI IRQ line 1 - 8	Disabled, Auto Select, 3, 4, 5, 6, 7, 10, 11, 12, 14 ,15	Select the IRQ number that should be used for this PCI interrupt line. Disabled – PCI INT not functional Auto Select – Let Bios decide which IRQ should be assigned 3, 4, 5, 6, 7, 10, 11, 12, 14, 15 – Use this IRQ number for the PCI interrupt **Note**: see chapter 5.1 for PCI IRQ Routing table

6.2.4.4.3 ICH USB Control Sub-Menu

Feature	Options	Description
USB Ports 0-5	Enabled 0-1 Enabled 0-3 Enabled 0-5	Enables USB controller Device 29
USB 2.0 Ports 0-5	Disabled, Enabled	USB Controller Device 29 EHCI functionality.
USB 2.0 Ports 6-7	Disabled, Enabled 6-7	Enables USB Controller Device 26
Legacy USB Support	Disabled, Enabled	Enable support for Legacy Universal Serial Bus.

6.2.4.5 ACPI Control Sub-Menu

Feature	Options	Description
Disable ACPI _Sx	None, S1, S2, S3, S4, S5	Select one of the ACPI power states: S1, S2, S3, S4, S5. If selected, the corresponding power state will be disabled.
Passive Cooling Trip Point	Disabled, 63 C, 71 C, 79 C, 87 C, 95 C	This value controls the temperature of the ACPI Passive Trip Point – the point in which the OS will begin throttling the CPU. Note: If the DTS is enabled, only values below 97C are valid.

Feature	Options	Description
Critical Trip Point	POR, 79 C, 87 C, 95 C	This value controls the temperature of the ACPI Critical Trip Point – the point in which the OS will shut the system off. Notes: (1)100C is POR for all Intels CPUs. (2) If value is > 100C and DTS is enabled, the Out-of-Spec Bit will be used. (3) The EC value will be set to 127 after ACPI initialation.
FACP – RTC S4 Flag Value	Disabled, Enabled	Valid only for ACPI Control the value for the RTC S4 flag in the FACP Table
FACP – PM Timer Flag Value	Disabled, Enabled	Valid only for ACPI Controls the timer used by the OS through the FACP Tables Flags. This is now possible with WINXP SP2 and beyond.
HPET Support	Disabled, Enabled	This field is valid only in the WindowsXP OS. Control the High Performance Event Timer through this setup option when enabled. The HPET Table will then be pointed to by the RSDT and the proper enable bits will be set.
HPET Base Address	0xFED00000, 0xFED01000, 0xFED02000, 0xFED03000	Select the Base Address for the High Performance Event Timer.

6.2.4.6 I/O Device Configuration Menu

Feature	Options	Description
Serial Port A	Disabled, Enabled, Auto	**Disabled** = Disabled the device **Enabled** = User configuration **Auto** = BIOS or OS chooses configuration
Base I/O address	3F8, 2F8, 3E8, 2E8	Set the base I/O address for Serial Port A.
Interrupt	3, 4	Set the interrupt for Serial Port A.
Serial Port B	Disabled, Enabled, Auto	**Disabled** = Disabled the device **Enabled** = User configuration **Auto** = BIOS or OS chooses configuration

Feature	Options	Description
Mode	Normal, IR, ASK-IR	Set the mode for Serial Port B (wired / infrared).
Base I/O address	3F8, 2F8, 3E8, 2E8	Set the base I/O address for Serial Port B.
Interrupt	3, 4	Set the interrupt for Serial Port B.

Warning: If you choose the same I/O address or Interrupt for more than one port, the menu displays an asterisk (*) at the conflicting settings.

6.2.4.7 Watchdog Options

Feature	Options	Description
Watchdog delay	1 second, 5 seconds, 10 seconds, 30 seconds 1 minute , 5 minutes, 10 minutes, 30 minutes	After watchdog is activated, he waits selected delay time before he starts counting the timeout period.
Watchdog timeout	0.4 second, 1 second, 5 seconds, 10 seconds, 30 seconds, 1 minute , 5 minutes, 10 minutes	Select the maximum watchdog trigger period. If the watchdog will not be triggered during selected period, system reset will be generated.
Watchdog start on boot	No, Yes	Select if the watchdog should be started at the end of POST.

6.2.4.8 AMT Sub-Menu

Feature	Options	Description
Intel AMT	Disabled, Enabled	Enable/Disable INTEL® Active Management Technology Bios Extension.
Platform Manageability	AMT	
Watch Dog Timer Config	Disabled, Enabled	Enable/Disable Watchdog Timer.
OS Timer Config	0	
Bios Timer Config	0	
AMT Wait Timer	Disabled, Enabled	Set timer to wait before sending ASF_GET_BOOT_OPTIONS
Intel AMT SPI Protected	Disabled, Enabled	Determine SPI ROM Lock enabled/disabled.
AMT CIRA Request Trigger	Disabled, Enabled	Set Trigger CIRA boot
AMT CIRA Timeout	0-255	Set “OEM defined timeout for MPS connection to be established.”
Mebx Debug Message	Disabled, Enabled	Mebx Debug Message Enabled/Disabled.
UnConfigure ME	Disabled, Enabled	Unconfigure ME without password Enabled/Disabled.
ME-IDE-R	Disabled, Enabled	
ME KT	Disabled, Enabled	
Console Redirection	Submenu	Additional setup menu to configure console

6.2.4.8.1 Console Redirection

Feature	Options	Description
Console Type	VT100, VT100 8bit, PCI ANSI, PCI ANSI 7bit, VT100+; VT-UTF8; ASCII	Enabled the specified console type
Continue C.R after Post	On, Off	Enables Console Redirection after OS has loaded.

6.2.5 The Security Menu

Feature	Options	Description
Supervisor Password	Displays Supervisor Password	Displays the current status of the Supervisor password (“Clear” or “Set”)
User Password	Displays User Password	Displays the current status of the User password (“Clear” or “Set”)
Set Supervisor Password	Press return to enter supervisor password	Supervisor Password controls access to the setup utility.
Set User Password	Press return to enter user password	User Password controls access to the system at boot.
Diskette Access	Supervisor, User	Controls access to diskette drives
Fixed disk boot sector	Normal, Write Protect	Write protects boot sector on hard disk to protect agains viruses
Password on boot	Disabled, Enabled	Enables password entry on boot
TPM Support	Disabled, Enabled	Enable Trusted Platform Module support.
Change TPM State	No Change, Enable, Disable, Activate, Deactivate, Clear, Enable & Deactivate, Deactivate & Disable, SetOwnerInstall with state=true, Set OwnerInstall with state=false	Changes TPM state.
Current TPM State	Displays Current TPM State	Displays the current TPM status.

6.2.6 The Power Menu

Feature	Options	Description
After Power Failure	Stay Off, Power On	Sets the mode of operation if an AC power loss occurs. Power On will turn the power on as soon as the power supply is back on. Stay Off will keep the power off until the power button is pressed.
PLL3 Spread Spectrum Mode	Off, On	Enables Spread Spectrum support for PLL3 in the CK 505 clock chip.
Spread Percentage	Down 0.5% Down 1.00% Down 1.50% Cntr 0.5% Cntr 1%	Select Spread Percentage for PLL3 in the CK505 Clock chip.
Hardware Monitor	Submenu	Configure Hardware Monitor

6.2.6.1 Hardware Monitoring Menu

Feature	Options	Description
CPU Vcore	Informative	Displays the current CPU voltage.
Supply Voltage (+12V)	Informative	Displays current supply Voltage for 12V.
CPU Temperature Sensor	Informative	Displays current CPU temperature.
Memory Temperature Sensor	Informative	Displays current Memory temperature.
Board Temperature Sensor	Informative	Displays current Board temperature.
FAN Speed	Informative	Displays the current fan speed.
Fan Control	Auto, Disabled	Fan Cruise Control Auto: Fan speed is automatically controlled by temperature Disabled: Fan set to maximum speed
Fan Speed Zone 2	30%, 40%, 50% Speed	Fan speed control for temperature zone 2 (Low temperature between 40°C and 50°C)
Fan Speed Zone 3	50%, 60%, 70% Speed	Fan speed control for temperature zone 3 (Medium temperature between 50°C and 60°C)

6.2.7 The Boot Menu

After you turn on your computer, it will attempt to load the operating system (such as DOS, Windows XP or Linux) from a device listed in the boot priority order. If it cannot find the operating system on that device, it will attempt to load it from the next device in that list.

Boot devices (i.e., with access to an operating system) can include: hard drives, floppy drives, CD ROMs, removable devices (e.g. USB sticks), and network cards.

Note: Specifying any device as a boot device on the Boot Menu requires the availability of an operating system on that device.

Selecting "Boot" from the Menu Bar displays the Boot menu, which looks like this:

Feature	Description
Boot priority order: 1: USB KEY: 2: USB FDC: 3: IDE CD: 4: USB CDROM: 5: IDE HDD: 6: 7: 8:	Boot priority order for next boot. System tries to boot the first bootable device in this list. Use <+> and <-> to change order. Use <x> to exclude or include device to boot priority list. <Shift >+<1> enables or disables a device <1-4> Loads default Boot sequence
Exclude from boot order: : USB HDD: : USB ZIP: : USB LS120: : PCI SCSI: : PCI BEV : Other USB: : PCI: : Legacy Network Card : Legacy : 1394 CDROM	System does not try to boot a device from this list.

Pressing the "F10" key during the bios boot phase will bring up the bios boot menu, which will allow you to select a different boot device for the current boot process only. In this boot menu, only devices in the "Boot priority list" will selectable. Devices excluded from boot order will not be shown.

6.2.8 The Exit Menu

The following sections describe each of the options on this menu. Note that <Esc> does not exit this menu. You must select one of the items from the menu or menu bar to exit.

Exit Saving Changes

After making your selections on the Setup menus, always select "Exit Saving Changes". This procedures stores the selections displayed in the menus in CMOS (short for "battery-backed CMOS RAM") a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS.

If you attempt to exit without saving, the program asks if you want to save before exiting. During boot-up, PhoenixBIOS attempts to load the values saved in CMOS. If those values cause the system boot to fail, reboot and press <F2> to enter Setup. In Setup, you can get the Default Values (as described below) or try to change the selections that caused the boot to fail.

Exit Discarding Changes

Use this option to exit Setup without storing in CMOS any new selections you may have made. The selections previously in effect remain in effect.

Load Setup Defaults

To display the default values for all the Setup menus, select "Load Setup Defaults" from the Main Menu.

If, during boot-up, the BIOS program detects a problem in the integrity of values stored in CMOS, it displays these messages:

System CMOS checksum bad - run SETUP Press <F1> to resume, <F2> to Setup

The CMOS values have been corrupted or modified incorrectly, perhaps by an application program that changes data stored in CMOS.

Press <F1> to resume the boot or <F2> to run Setup with the ROM default values already loaded into the menus. You can make other changes before saving the values to CMOS.

Discard Changes

If, during a Setup Session, you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you previously saved to CMOS.

Selecting "Discard Changes" on the Exit menu updates all the selections with their previous values.

Save Changes

Selecting "Save Changes" saves all the selections without exiting Setup. You can return to the other menus if you want to review and change your selections.

6.3 Bios Update

If a System-BIOS update is required please follow these instructions:

1.) Create a bootable DOS disk/usb-stick/hdd.
2.) Copy PHLASH16.EXE, BIOS.WPH and UPDATE.BAT to this device.
3.) Boot the system from this device.
4.) Type "update.bat" to update the System BIOS.
5.) When the BIOS update has finished, reboot the system.

Note: After the system has been updated, the CMOS has been changed to defaults and therefore it is necessary to enter Setup (press F2 at boot time) to configure the system settings.

6.4 Bios Crisis Recovery

Should the BIOS setup be altered, such that it is no longer possible to re-enter the BIOS setup – for example if wrong display selected, the following methods can be used to restore the default settings:

1. Blind reset to defaults
2. Crisis recovery / clear backup EEPROM jumper
3. Crisis recovery software (usually only necessary if the BIOS is corrupted – for example if power was removed during a BIOS update)

6.4.1 Blind Reset to defaults

In the event that there is no display or the display is for some reason not active, in order to get the BIOS back to the default settings (and so enable the display) the following sequence must be performed :

1. During boot press F2 to get into BIOS setup (F2 can be pressed repeatedly, at least until the numlock LED on Keyboard is on)
2. Press F9 and then enter to reset to default settings
3. Press F10 and then enter to save and exit the BIOS setup
4. System should then reboot with the default settings.

6.4.2 Crisis Recovery / Clear backup EEPROM Jumper

See Jumper Section 3 to find the Crisis Recovery or Clear backup EEPROM Jumper.

The two pads of this jumper should be shorted (using tweezers or pliers) before applying power to the board and held shorted until the crisis recovery has started. As soon as crisis recovery is started the short can be removed.

The programming process is signalled by short beeps and terminated after successful programming with one long beep. After that, the system is automatically rebooted.

6.4.3 Crisis Recovery software

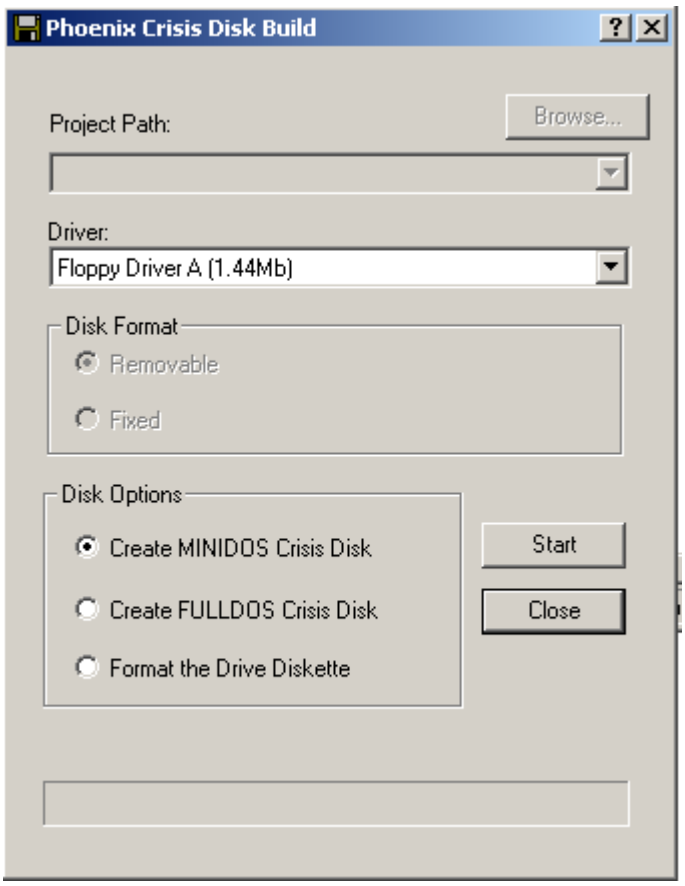
This technique should only be required in the event of a serious corruption of the BIOS – for example following an unsuccessful attempt to update the BIOS

To use this technique a special software – CRISDISK and a USB dongle must be obtained from MSC.

Note: Contact the MSC customer support for information how to obtain the CRISDISK.ZIP software and the USB recovery dongle.

Please follow these simple steps to create a bootable crisis recovery medium:

1. Unzip CRISDISK.ZIP and start the windows-based program WINCRIS.EXE on the host system. A window will pop up as shown below:



2. In the drop-down box, select either "Floppy Drive A" to create a recovery disk, or select "Removable Disk 0 (xxxMb)" to create a recovery USB stick. Disk options should be left as "Create MINIDOS Crisis Disk".

3. Press the start button to generate the selected crisis recovery medium.

Proceed as follows to use the generated Disk or USB stick for the recovery :

Plug the USB dongle into a free USB port on the failing system before switching the system on. Please make sure that you use different USB controllers for USB dongle and USB crisis recovery medium. After power-up, crisis recovery mode should start automatically.

The programming process is signalled by short beeps and terminated after successfull programming with one long beep. After that, the system is automatically rebooted.

Important Notes:

- USB recovery dongle and USB crisis recovery device must not be plugged to the same USB controller.
- Crisis recovery may take up to 5 minutes
- A long beep indicated successful recovery
- Crisis recovery does not include the bootblock.